Memristor-based Random Access Memory:

The delayed switching effect could revolutionize memory design

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***Abstract*— Memristor's on/off resistance can naturally store binary bits for non-volatile memories. In this work, we found that memristor's another peculiar feature that the switching takes place with a time delay (we name it "the delayed switching") can be used to selectively address any desired memory cell in a crossbar array. The analysis shows this is a must-be in a memristor with a piecewise-linear φ-q curve. A "circuit model"-based experiment has verified the delayed switching feature. It is demonstrated that memristors can be packed at least twice as densely as semiconductors, achieving a significant breakthrough in storage density.**

Keywords- memristor; delayed switching; Random Access Memory (RAM)

I. INTRODUCTION

Memristor (a contraction of "memory resistor") is a passive two-terminal circuit element that maintains a functional relationship between magnetic flux and electric charge. Memristor theory was formulated and named by Leon Chua in a 1971 IEEE Transaction paper titled "Memristor—The Missing Circuit Element" [1]. Chua strongly believed that a fourth device existed to provide conceptual symmetry with the resistor, inductor, and capacitor. This symmetry follows the observation that a basic passive circuit element links two of the four fundamental circuit variables, namely voltage, current, charge and flux. A memristor device linking charge and flux (time integrals of current and voltage) was predicted by Chua at the time. Chua also used memristor to model an Amorphous "Ovonic" threshold switch and an electrolytic E-cell, process many types of signals and generate various waveforms such as staircase waveform [1].

37 years later, in May 2008, a team at HP Labs led by R. Stanley Williams announced the discovery of an memristor based on a nano-scale thin film of titanium dioxide, which was presented in a Nature paper titled "The missing memristor found"[2]. The HP device is composed of a thin (5 nm) titanium dioxide film between two electrodes. The oxygen vacancies act as charge carriers. When an electric field is applied, the oxygen vacancies drift, changing the boundary between the non-depleted high-resistance and depleted low-resistance layers. Thus the resistance of the film as a whole is dependent on how much charge has been passed through it in a particular direction, which is reversible by changing the direction of current [2].

In addition to the above HP device, there were the following claims to have developed other types of memristors: (1) Spin memristive systems [3]; (2) Polymeric memristor [4]; (3) Manganite memristive systems [5]. These claimed memristors broaden the possible range of memristors.

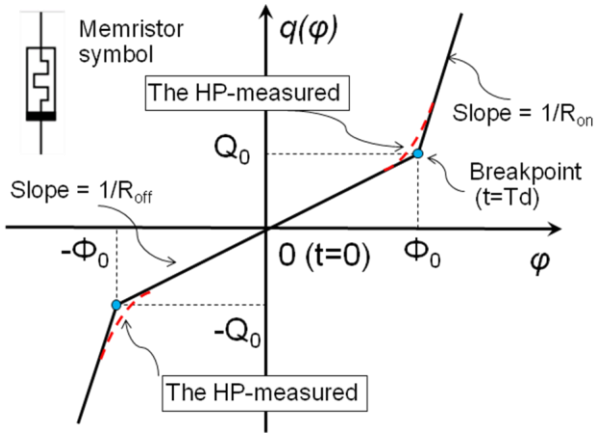

Fig.1 A memristor links electric charge, q, and magnetic flux, φ. A freezing memory property can be seen: a memristor stores either off resistance (Roff) or on resistance (Ron) value. It is assumed that φ = 0 & q = 0 at time t = 0. A dotted curve having a continuous derivative shows the actually measured φ-q curve of a HP nano-scale titanium dioxide memristor [2]. The solid piecewise-linear curve approximates the HP-measured one. As will be demonstrated later, so-called "delayed switching" feature is a must-be of this piecewise-linear φ-q curve.

II. A PREVIOUS DESIGN OF MR-RAM WITH MEMRISTOR/TRANSISTOR-PER-CELL

Naturally, the freezing memory property that a memristor stores resistance value suits memristors for computer memory. As shown in Fig.1, a memristor is featured with two stable states: off resistance (R_{off}) and on resistance (R_{on}). The resistance stays constant whether we turned off the voltage. To demonstrate the significance of our work of using the so-called

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delayed switching property, we pause to present our previous design of Memristor Random Access Memory (MR-RAM) with Memristor/Transistor-per-Cell [6].

Resembling Dynamic Random Access Memory (DRAM), we designed an MR-RAM architecture as shown in Fig.2, in which memristors replace capacitors in a DRAM [7]. This MR-RAM is arranged in a square array of one memristor and one transistor (or a MOSFET switch) per cell. The illustration shows a simple example with only 2 by 2 cells.

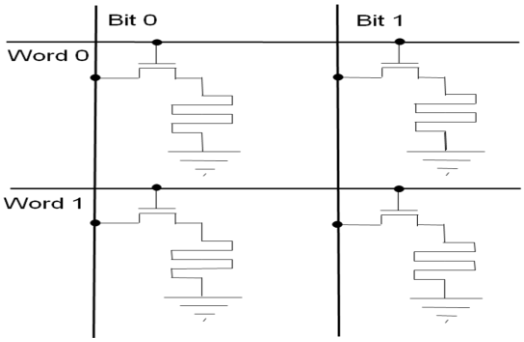

Fig.2 Design of Random Access Memory with Memristor/Transistor-per-Cell [6]. To write/read a desired memristor cell, the corresponding transistor is opened by energizing a word line and a bit line.

To write to MR-RAM, the row is opened and a given bit line charges the memristor to the desired value. Refresh logic is commonly used with DRAMs to automate the periodic refresh. This makes the DRAM circuit more complicated. In MR-RAM memristors consume much less power as a regular refreshing procedure (otherwise the stored charge will be lost) is not needed. Furthermore, a memristor/transistor per cell takes a much less area compared with the 4-6 transistors per cell architecture in a Static Random Access Memory (SRAM) [7].

In the proposed MR-RAMs [6], diode or transistor current rectification is desirable to reach readout operation. As shown in Fig. 2, the basic array cell is a transistor (selective component) connected in series with a memristor junction (storage component). In the absence of such transistors all the memristors at each intersection of every bit and word line in the cross-point array would otherwise be electrically connected to one another.

However, such a memristor-transistor series still puts a severe constraint on the storage density. The area of a transistor is much larger than a simple two-terminal memristor. In this work, our original contribution is to take full advantage of so called delayed switching property of a memristor and design a transistor-free Memristor-based RAM (MR-RAM) architecture. It comprises two sets of conductive lines, an array of memristors (only) at each intersection, and a peripheral circuitry. Such a simplified transistor-free architecture described in this paper overcomes the transistor-area constraint in the prior art and achieves a significant breakthrough in storage density.

III. DELAYED SWITCHING PROPERTY OF MEMRISTORS

Conceptually, a memristor element links electric charge, q, and magnetic flux, φ [1][8][9]. This is a missing link in the pairwise mathematical equations that relate the four circuit quantities – charge, current, voltage and magnetic flux – to one another. The φ-q curve of a memristor is already shown in Fig.1. The v-i plot demonstrates hysteresis (not shown here) and the flux-charge (φ-q) plot in Fig.1 shows that the charge is a single-valued function of the magnetic flux. A breakpoint in the φ-q curve breaks the curve into two linear pieces: off resistance (R_{off}) and on resistance (R_{on}). It is assumed that $\varphi = 0$ & $q = 0$ at time $t = 0$. A dotted curve having a continuous derivative shows the actually measured φ-q curve of a HP nano-scale titanium dioxide memristor [2]. The solid piecewise-linear curve with zero switching time approximates the measured one with a finite switching time.

In a delayed switching test, a voltage V_s(t) is applied to the memristor and a current $i(t)$ is imposed. $M(q) = d\varphi/dq$ has the unit of resistance and in the case where the φ-q curve is straight lines (a piecewise linear model), we obtain $M(q) = R_{off}$ or R_{on} that is a constant. In other words, a memristor behaves like an ordinary resistor at a given instant of time t_0, its resistance depends on the complete past history of the memristor current (voltage), i.e. the time integral of the current (voltage) from $t = -\infty$ to $t = t_0$.

$$q(t) = \int i(t)dt = \int \frac{E \cdot dt}{M} = \frac{E}{M} \cdot t \qquad (1)$$

At the breakpoint where $t = T_d$, we have $q(T_d) = Q_0$ and $\varphi(T_d) = \Phi_0$. Therefore

$$Q_0 = \frac{E}{\frac{\phi_0}{Q_0}} \cdot Td \qquad (2)$$

$$T_d = \frac{\phi_0}{E} \qquad (3)$$

Fig.3 shows a memrisor's current waveforms corresponding to the square-wave pulses with amplitude E, $E/2$. These waveforms are rather peculiar and certainly not typical of those normally observed in RLC circuits. A delayed switching property is observed: the switching from the high resistance (R_{off}) to the low resistance (R_{on}) takes place with a time delay T_d after the application of an input square-wave voltage (Fig.3(a)). The time delay T_d increases as the amplitude E of the square-wave pulse $V_s(t)$ decreases, as described in Eq.(3). If the input voltage is removed before the switching takes place, i.e. the width T of the input voltage pulse is smaller than

T_d, the memristor keeps unaltered (Fig.3(b)). Therefore T should be chosen in such a way that $T_d < T < T'_d = 2T_d$.

This property shown in Fig.3 results from the piecewise-linear nature of the assumed φ-q curve in Fig.1. The abrupt jump is due to zero switching time. "Full selection" in Fig.3(a) means a full voltage, E, is applied across the memristor. "Half selection" in Fig.3(b) means only a half voltage, $E/2$, is applied.

The current amplitudes through the memristor are given by

$$i_1 = \frac{E}{R_{off}} \tag{4}$$

$$i_2 = \frac{E}{R_{on}} \tag{5}$$

where R_{off} and R_{on} represent the mem-resistance corresponding to pieces 1,2 of the memristor φ-q curve and where (Q_0, Φ_0) is the coordinate of the breakpoint between these two pieces (at the breakpoint $t = T_d$).

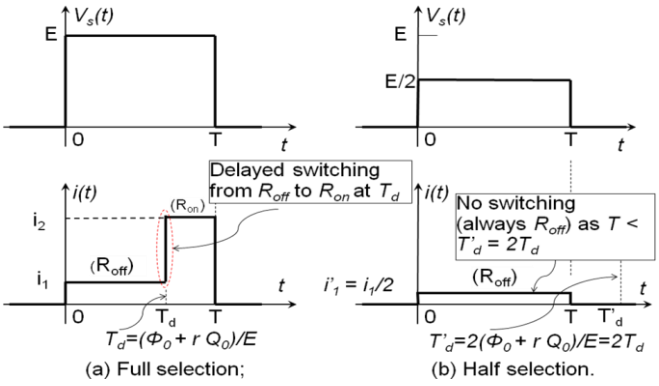

Fig.3 The memrisor's delayed switching property: the switching from one resistance state to another due to an input pulse takes place with a time delay T_d. T_d increases as the amplitude E of the square-wave pulse, $V_s(t)$, decreases.

The abrupt jump in Fig.3 is due to zero switching time. In practice, it always takes a finite but small time interval for a memristor to switch completely from a high resistance to a low resistance or vice verse. This can also be modeled by replacing the assumed φ-q curve with the actually measured one as shown in Fig.4(a). The only discrepancy between the waveforms in Fig.4(b) and the one in Fig.3(a) is that the rise (fall) time is not zero any longer. Nevertheless, the memrisor's delayed switching property still persists as long as $T_{d2} < 2T_{d1}$. T is chosen in such a way that $T_{d2} < T < 2T_{d1}$.

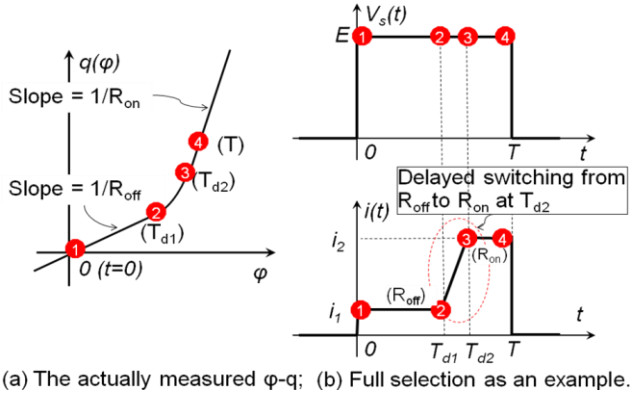

Fig.4 In practice, it always takes a finite but small time interval for a memristor to switch completely from a high resistance to a low resistance or vice verse. The number 1-4 label successive time points during a square wave period T.

The piecewise-linear nature manifests itself vividly in the form of a delayed switching property that the switching versus a square-wave input takes place with a time delay. In other words, it is a must-be in a memristor with a piecewise-linear φ-q curve. The physical interpretation of this phenomenon is that the element possesses certain inertia, i.e. electric charge q or magnetic flux φ is inertial with the tendency to remain unchanged (settle to some equilibrium state). It cannot respond as rapidly as the fast variation in the excitation waveform and always takes a finite time interval for a memristor to change its resistance value. The number 1-4 label successive time points during a square wave period T in Fig.4.

IV. Circuit-Model Experiments of Delayed Switching Effect

A number of exemplified memristors, as mentioned in Section 1, broaden the possible range of memristors. There are still skeptics arguing against the HP device [2] that is thought not to be a fourth fundamental circuit element [10] as it used a chemical mechanism to achieve a resistance dependent on the history of current [8]. The HP device neither uses magnetic flux as Chua's hypothetical memristor suggested [1], nor stores charge as a capacitor does [9]. The HP scientists themselves recognized that the HP device did not actually involve magnetism and the integral over the voltage reflected how far the dopants had moved and thus how much the resistance of the device had changed [2]. The interesting point is whether one can bypass magnetic interaction but still satisfy Chua's definition [10].

In this section, we will use Chua's "circuit-model" [1][8] to construct a synthesized memristor to actually measure its delayed switching property and the behavior of a memristor in a full selection operation and a half selection operation, respectively. The advantages of using a synthesized memristor include a broad generalization of memristors to an interesting class rather than a specific element and the ease of changing the parameters.

According to Chua's "circuit-model" theory, a memristor with any prescribed φ-q curve can be realized by using an active circuit in connection with an appropriate nonlinear element [1][8]. In Fig.5, the V-I curve of a diode connected in Port 2 (v_2, i_2) is transformed into the φ-q curve of a synthesized memristor in Port 1 (v_1, i_1).

To demonstrate the delayed switching property possessed by the synthesized memristor shown in Fig.5, a oscilloscope is used to trace the voltage $v(t)$ and current $i(t)$ of the memristor. The Zener diode BZX79C is with a forward voltage of 0.8 V. The waveforms $v(t)$ and $i(t)$ in Fig.6(a) (Half selection, an input voltage of 10 mV) and Fig.6(b) (Full selection, an input voltage of 20 mV) are measured with a 10 kHz square-wave input signal. A delayed switching is clearly seen in Fig.6(b). The corresponding V-I curve is also measured, as shown in Fig.6. It is interesting to observe that the delayed switching property of a memristor results from the piecewise-linear nature of its φ-q curve (Fig.5).

As predicted by Chua [1][8], a finger-print of a memristor is its zero-crossing property. Observe that in spite of the memory effect which normally introduces phase shifts in conventional memory systems (e.g. a capacitor memory), the output of a memristor is zero whenever the input is zero and hence the input-output v-i figure always passes through the origin, as shown in Fig.6. The v-i curves reflect the delayed switching behaviour of the memristor: it begins with a high resistance, and as the voltage increases, the currently slowly increases. As the breakpoint is overtaken, the resistance drops, and the current increases more rapidly with increasing voltage until the maximum is reached. Then, as the voltage decreases, the current decreases but more slowly. When the voltage turns negative, the resistance of the device increases, the resistance increases, resulting in an symmetric switching loop.

The amplitude/frequency response of a memristor is especially interesting to a practical memory application. As shown in Fig.6, as the excitation amplitude decreases or equivalently the excitation frequency increases toward $T < T_d$, the Lissajous V-I figure shrinks and tends to a straight line passing through the origin. This implies that the hysteretic effect of a memristor decreases as the voltage amplitude decreases (equivalently frequency increases) and hence it eventually degenerates into a purely resistor with a single resistance value (no switching).

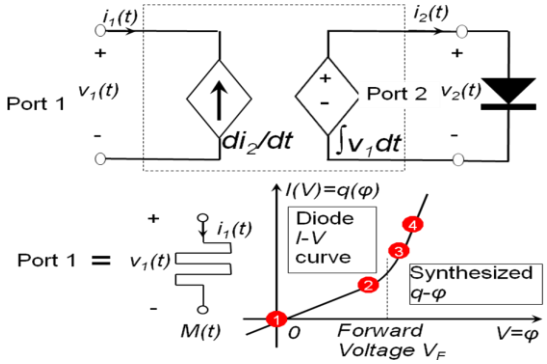

Fig.5 Circuit realization of a memristor using controlled active sources and a diode. The circuit is equivalent to a memristor with the shown φ-q curve that is transformed from the diode's V-I curve.

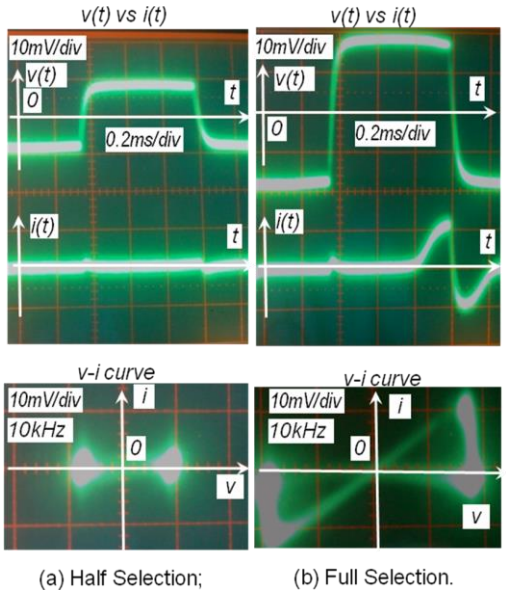

Fig.6 Measured waveforms v(t)-i(t) and v-i curve for Half Selection (a) and Full Selection (b). A delayed switching is clearly seen in Full Selection. The v-i figure always passes through the origin. As the voltage amplitude decreases, the v-i curve degenerates into a purely resistor with a single resistance value (no switching).

V. TRANSISTOR-FREE MEMRISTOR RANDOM ACCESS MEMORY (MR-RAM)

The peculiar property of delayed switching inspires us to apply it to a novel transistor-free crossbar architecture for MR-RAMs, as shown in Fig.7. The architecture comprises two sets of conductive lines, an array of memristors at each intersection.

Write operation of switching the memristor from one resistance state to another with conductor currents is associated with activations of the corresponding word line and bit line. When $\pm E/2$ are applied to a word line and a bit line, respectively, the combined voltages drop E at the intersection of the energized word and bit lines will switch the resistance state of the memristor located at the intersection (Full selection). "Half selection" occurs when a memristor cell is selected by only one word line or bit line. Obviously, those so-called half-selected memristors should not be written (altered). "Half selection" means only a half voltage, $E/2$, is applied, as shown in Fig.7. It is possible to write simultaneously all the bits in a word by energizing a single word lines and all the bit lines. The ground of the un-selected lines ensures that those cells in contact with the un-energized word and bit lines have zero voltage drop and do not conduct, otherwise the leakage currents may alter the resistance state of those un-desired cells by mistake. The above operation is based on an assumption that the lead resistance is negligible. If the lead line resistance

is not small compared to that of the memristor elements then the voltage distribution along the chosen line will appear. Such a voltage distribution will possibly cause leakage currents through the memristors. As will be shown in Fig.10, low-resistance shorting bars are used between cells to reduce the lead line resistance.

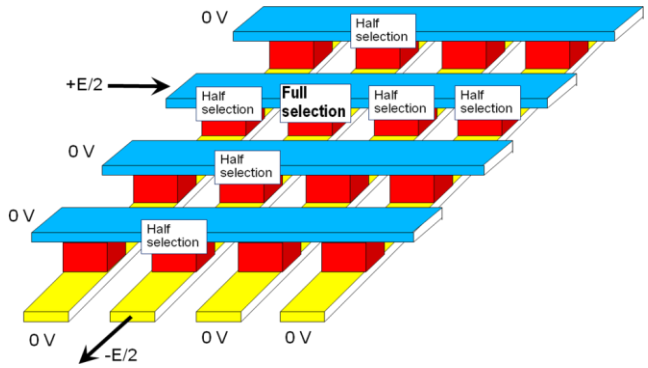

Fig.7 The crossbar architecture. "Full selection" means a full voltage, E, is applied across the two wires with the desired memristor at the intersection. "Half selection" means only a half voltage, E/2, is applied across the (undesired) memristor.

Read operation of measuring the value of any individual memristor resistance to determine ''0'' or ''1'' becomes a very difficult task due to the mutual electrical connection between all the memristors, referring again to Fig.7. Any direct measurement would result in unavoidably introducing the contribution from the rest of the resistors. Similar to a diode-free Magnetic RAM architecture we used in [11], this difficulty would be overcome by introducing a concept of ''virtual ground'' of operational amplifier. Referring now to Fig.8, since the input impedance of an operational amplifier is considered very high or even infinite, no current can flow into or out of the inverting input terminals, thus this point is at 0 V, commonly referred to as virtual ground. In an example of read operation a voltage across the selected Bit_{11} under a read condition is established by setting the selected Word line 1 to an input voltage excitation V_{in}. The bit line 1 is clamped to virtual ground 0 V, by setting the electronic switch K_1 (one switch per column, occupying a very small silicon area) to read mode, to create the voltage across the selected Bit_{11}. The bit line 0 is clamped to actual ground 0 V by setting the switch K_0 to standby mode. The unselected Word line 0 remains at the standby voltage level, *0 V*. Although there are a large number of possible current paths in the cross-point organization, no ambient current path, except the dotted path I_s through the chosen Bit_{11}, exists because all the bit lines are set to virtual or actual ground. Thus the unselected Bit_{00}, Bit_{01} have zero voltage drop and do not conduct. The unselected Bit_{10} conducts but does not contribute to the read output.

The resistance state of the memory cell is detected or read by applying a voltage (with a much smaller amplitude than the write one for power saving) across the selected memristor and measuring the current through the memristor. In the bit line control circuitry this current is converted to a voltage V_{out} to read the datum stored in selected Bit_{22}. The operational amplifier has its noninverting input terminal brought to ground. As mentioned above, no current can flow into or out of the inverting input terminal. This forces I_s to flow through the feedback resistor R_f to produce a sense voltage V_{out} at the output terminal. The read signal gain is equal to the ratio between R_f and M. The low resistance state (R_{on}) and high resistance state (R_{off}) of M_{ij}, at the intersection of the ith word line and the jth bit line, produce different values of sense current I_s in inverse proportion and therefore different values of output voltage V_{out}. The MATLAB simulation result is shown in Fig.9. The output voltage V_{out} has two discrete values. While not shown in Fig.8, the output voltage V_{out} will be compared to a reference voltage level set to a value halfway between the expected values for the two possible states of the memory cell and the difference will be amplified further to provide full logic levels. After the data are read, the voltage on Word line 2 is returned to the standby value. The resistance state remains unchanged after the read operation.

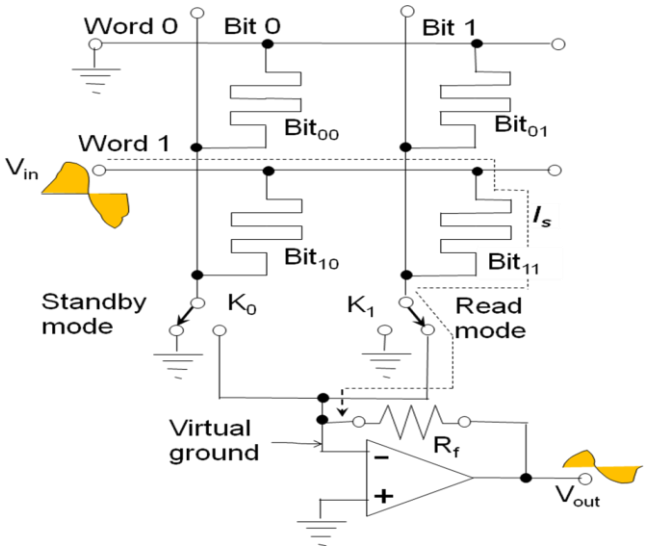

Fig.8 Read operation in a 2x2 bit transistor-free MR-RAM. Although there are a large number of possible current paths in the cross-point organization, no ambient current path, except the dotted path Is through the chosen Bit_{11}, exists. This is due to the virtual ground concept of an operational amplifier.

The above read operation would slightly alter the resistance of the read memristor cell. In order to realize a non-destructive readout, at the 2nd phase of a read cycle, the resistance value is restored by applying an opposite voltage pulse as shown in Fig.8 (for example, a cell's resistance would be read with an alternative voltage so that they do not affect the stored value).

We establish a coupled variable-resistor model for a typical memristor in MATLAB (R2008b) [12]. Fig.9 depicts a non-destructive readout in which a sinusoidal excitement is applied. The resistance fluctuates between $R_{on} = 1\ \Omega$ and $R_{off} = 160\ \Omega$ (When enough charge has passed through the memristor that the ions can no longer move, the element

ceases to integrate $q = \int idt$ but rather keeps at an upper bound). It is proven that a memristor remembers the voltage (current) history, i.e. the resistance holds even after the voltage/current is removed.

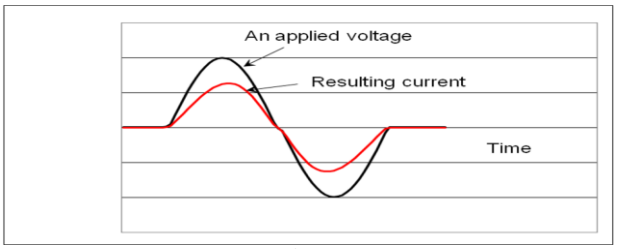

Fig.9 A non-destructive read mode for MR-RAM is designed to restore the altered states.

VI. MR-RAM CHARACTERIZATION

Our objective in this section is to give the characterization of MR-RAMs, especially the highest storage density, the maximum working frequency, the heat dissipation and their relationships. Some characteristics are to be found unique due to memristor's peculiar features.

6.1 Integration Density of MR-RAM

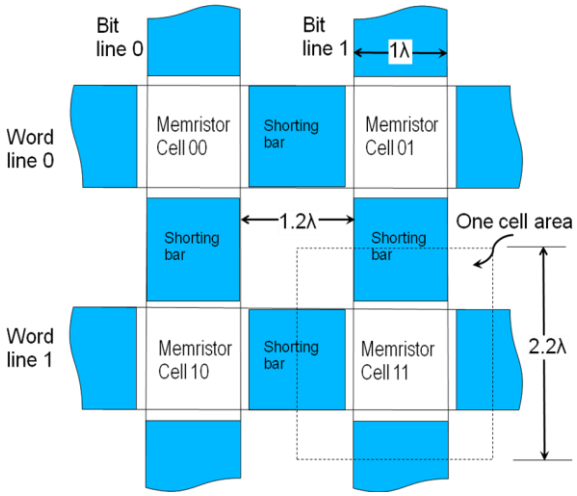

Fig.10 An areal view of a 2x2 bit MR-RAM with low-resistance shorting bars running between cells. λ is the resolution limit of the lithography used to fabricate the memory cells. The minimum line width is λ and the minimum distance between lines is 1.2 λ, thus one cell area is $4.84\lambda^2$.

Fig.10 is an areal view of a *2x2* bit MR-RAM showing a cell area of $4.84\lambda^2$, where λ is the resolution limit of the lithography used to fabricate the memory cells. At the moment, λ is unlikely to reduce below *4 nm* [13], unless there is significant progress in photolithography technology. The HP device displays fast ion conduction in a TiO_{2-x} junction sandwiched by a pair of *40-50 nm* platinum wires, it is considered a nanoscale device [2]. HP also reported that the resistance of their memristors is more significant at the nanometer scale than it is at the micrometer scale [2], which is good news to realize an Ultra-Dense Memristor Memory. The minimum line width is λ and the minimum distance between lines is *1.2* λ (low-resistance shorting bars are placed between cells), thus one cell area is $4.84\lambda^2$. Compared with more than $10\lambda^2$ for minimum-size Dynamic RAM (DRAM) cells [14][15], MR-RAM potentially can be at least twice as dense. Essentially, MR-RAM is a permanent information storage technology (non-volatility) whereas Dynamic RAM (1 transistor per cell with refreshing regularly) or static RAM (4-6 transistors per cell) [7] is not. The comparison is summarized in Table 1.

Table 1 Comparison of MR-RAM and semiconductor memory.

	Transistor-free MR-RAM	*Semiconductor Memory*
Fabrication	*Simple structure (2 ~ 3 masks)*	*Complicated structure (10 ~ 20 masks)*
Density	*Minimum cell area: $4.84\lambda^2$*	*Minimum cell area: $10\lambda^2$ (DRAM)*
Non-volatility	*yes*	*no*

6.2 Working frequency of MR-RAM

The maximum working (write) frequency f_{max} of MR-RAM is given by $1/T_d$.

$$f_{\max} = 1/T_d = \frac{E}{\phi_0} \qquad (6)$$

It is apparent that the (write) working frequency increases with increased voltage. However an analogous interpretation may be that the increased voltage consumes more power, eventually limiting the frequency increase. This will be discussed in details in Section 6.3.

It is also observed that the (write) working frequency increases with decreased Φ_0. Small Φ_0 means the breakpoint of the φ-q curve of a memristor should be close to the origin, which represents the material requirements for memristors fabrication. Another material requirement for memristor fabrication is the off-to-on resistance ratio that represents the signal-noise ratio of a memory device. Modern transistors have an off-to-on resistance ratio of 10,000 to 1 [13]. The HP titanium dioxide memristor has an off-to-on resistance ratio of 160~380 to 1 [2]. HP thought a resistance ratio of at least 1,000 to 1 is needed to get a high-performance memory [13]. Large off-to-on resistance ratio means the φ-q curve of a memristor should have a sharp breakpoint (with an abrupt slope change across the breakpoint) rather than a smooth one.

6.3 Heat Dissipation of MR-RAM

The heat dissipation during a write operation (a single switching event during $[0, T=T_d]$ as shown in Fig.3(a) for "Full selection") can be obtained by

$$Heat_{FullSelection} = \int_0^{T_d} i(t)v(t)dt = \int_0^{T_d} \frac{v(t)^2}{M(q(t))}dt =$$

$$= E^2 \int_0^{T_d} \frac{dt}{M(q(t))} = E^2 \int_0^{Q_0} \frac{dq}{i(q)M(q)} = E^2 \int_0^{Q_0} \frac{dq}{v(q)} = EQ_0 \quad (7)$$

where it is assumed that the applied voltage remains constant (E as shown in Fig.3) and for a memristor to switch from $q(t=0)=0$ to $q(t=T_d) = Q_0$ in time 0 to T_d.

Similarly, the heat dissipation for "Half selection" (Fig.3(b)) can be obtained by

$$Heat_{HalfSelection} = \frac{1}{4} EQ_0 \quad (8)$$

The total heat dissipation for an m x n array of memristors (one write operation) is then given by

$$Heat_{Total} = 1 \times Heat_{FullSelection} + [(m-1)+(n-1)] \times Heat_{HalfSelection} =$$
$$= [1 + \frac{1}{4}(m+n-2)]EQ_0 \quad (9)$$

In a read operation, a much smaller voltage (than a write voltage) will be used to measure the resistance; therefore the heat dissipation for read operations is negligible.

Substituting Eq.(6) into Eq.(9), we have the maximum working frequency

$$f_{\max} = \frac{Heat_{\max}}{[1 + \frac{1}{4}(m+n-2)]Q_0\phi_0} \quad (10)$$

where $Heat_{max}$ is the maximally allowed heat dissipation for the memory chip.

Section 6.2 gives an analogous interpretation that the (write) working frequency increases with increased voltage that consumes more power, eventually limiting the frequency increase. This accurate relation is now described in Eq.(10), which implies that the maximum working frequency is constrained by the maximally allowed heat dissipation for the MR-RAM chip and the number of memristor cells in the chip. The higher the maximally allowed heat dissipation, the higher the working frequency. The more memristor cells a MR-RAM chip contains, the lower the working frequency. Writing a desired memristor cell has to involve some other memristor cells thereby generating more heat and limiting the frequency of the write itself. This may be a major drawback of this Transistor-free MR-RAM architecture. Nevertheless, one should note that a regular refreshing procedure in a DRAM could involve all the memory cells and a DRAM is even not non-volatile.

Eq.(10) also suggests that the smaller Q_0 and Φ_0 the higher the frequency. This represents a material requirement for memristor fabrication that the breakpoint of the φ-q curve of a memristor should be close to its origin.

VII. RESULTS

We make a step forward in future practical applications of the memristor concept by designing a Transistor-free Memristor-based Random Access Memory (MR-RAM) architecture to enable a nanoscale computer. This work is the first of its kind in terms of using memristor's unique delayed switching feature to address the desired memristor cell from a two-dimensional array. It is found that the mixture of the freezing memory property and the delayed switching property makes memristor a perfect candidate for ultra-dense RAMs owing to its simple architecture without using any traditional selective component such as diode or transistor. In such a design, memristors consume much less power as a memristor is non-volatile. An analytical model shows memristors can be packed at least twice as densely as semiconductors, achieving a significant breakthrough in storage density. The hysteresis degeneration due to the low amplitude and the relationship between the maximum working frequency and the heat dissipation are investigated. Some characteristics are found unique due to memristor's peculiar features. A non-destructive read mode for MR-RAM is also designed to restore the altered states.

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