University of Kent

Kent Academic Repository

Meraj, Sheikh Tanzim, Hasan, Mohammad Kamrul, Islam, Jahedul, El-Ebiary, Yousef A. Baker, Nebhen, Jamel, Hossain, Md. Moinul, Alam, Md. Khorshed and Vo, Nguyen (2021) ***A Diamond Shaped Multilevel Inverter With Dual Mode of Operation.*** **IEEE Access, 9 . pp. 59873-59887.**

Downloaded from

https://kar.kent.ac.uk/87994/ The University of Kent's Academic Repository KAR

The version of record is available from

https://doi.org/10.1109/ACCESS.2021.3067139

This document version

Publisher pdf

DOI for this version

Licence for this version

CC BY (Attribution)

Additional information

Versions of research works

Versions of Record

If this version is the version of record, it is the same as the published version available on the publisher's web site. Cite as the published version.

Author Accepted Manuscripts

If this document is identified as the Author Accepted Manuscript it is the version after peer review but before type setting, copy editing or publisher branding. Cite as Surname, Initial. (Year) 'Title of article'. To be published in ***Title of Journal*** , Volume and issue numbers [peer-reviewed accepted version]. Available at: DOI or URL (Accessed: date).

Enquiries

If you have questions about this document contact ResearchSupport@kent.ac.uk. Please include the URL of the record in KAR. If you believe that your, or a third party's rights have been compromised through this document please see our Take Down policy (available from https://www.kent.ac.uk/guides/kar-the-kent-academic-repository#policies).

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 18, 2021, accepted March 9, 2021, date of publication March 18, 2021, date of current version April 26, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3067139

A Diamond Shaped Multilevel Inverter With Dual Mode of Operation

SHEIKH TANZIM MERAJ[1], MOHAMMAD KAMRUL HASAN[2], (Senior Member, IEEE), JAHEDUL ISLAM[3], YOUSEF A. BAKER EL-EBIARY[4], (Member, IEEE), JAMEL NEBHEN[5], MD. MOINUL HOSSAIN[6], (Member, IEEE), MD. KHORSHED ALAM[1], (Student Member, IEEE), AND NGUYEN VO[7]

[1]Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Seri Iskandar 32610, Malaysia
[2]Faculty of Information Science and Technology, Universiti Kebangsaan Malaysia (UKM), Bangi 43600, Malaysia
[3]Department of Fundamental and Applied Sciences, Universiti Teknologi PETRONAS, Seri Iskandar 32610, Malaysia
[4]Faculty of Informatics and Computing, University Sultan Zainal Abidin (UniSZA), Kuala Terengganu 21300, Malaysia
[5]College of Computer Science and Engineering, Prince Sattam Bin Abdulaziz University, Alkharj 11942, Saudi Arabia
[6]School of Engineering and Digital Arts, University of Kent, Canterbury CT2 7NT, U.K.
[7]Department of Information Technology, Victorian Institute of Technology, Melbourne, VIC 3000, Australia

Corresponding authors: Mohammad Kamrul Hasan (mkhasan@ukm.edu.my) and Yousef A. Baker El-Ebiary (yousefelebiary@unisza.edu.my)

This work was supported by the Universiti Kebangsaan Malaysia under Grant FRGS/1/2020/ICT03/UKM/02/6 and Grant GGPM-2020-028.

ABSTRACT This study presents a novel multilevel inverter structure that can operate in both switched capacitor and asymmetric DC source modes. In the first mode, it can produce seven-level output voltage employing two switched capacitors and one single DC supply. The five-level output voltage is produced while operating the second mode. The voltage ratio between the input and output voltage for the capacitor mode is 1:3 (triple voltage gain). During the first mode, the capacitor of the inverter is self -balanced whereas the inverter can produce higher voltage output in the DC source mode. The proposed inverter reduces the total standing voltage in both modes of operations as it can generate the output voltage without requiring any additional H-bridge circuit. The feasibility and predominate features of the proposed inverter have been established by comparing with existing topologies in terms of power components count. Results obtained from this study are validated using simulation employing sinusoidal pulse width modulation (SPWM). A hardware prototype has also been developed for further validation.

INDEX TERMS Asymmetric inverter, boost inverter, multilevel inverter, power electronics, switched capacitor, SPWM.

I. INTRODUCTION

Multilevel inverters (MLIs) have emerged as a perfect solution in the field of low and medium power applications by providing better power quality for DC to AC power conversion. Besides, multilevel inverters possess other exceptional characteristics such as reducing total harmonic distortion, utilizing less number of power equipment, decreasing common-mode voltage, etc. [1]. Another significant feature of MLIs is that it can generate a higher output voltage without imposing high voltage stress on semiconductor switches. Therefore, the MLIs are highly reliable for various applications in the field of power engineering such as energy balancing circuits [2], static synchronous compensator (STATCOM) [3], electric vehicles, high voltage DC systems (HVDC) [4] and so on. In terms of renewable energy applications, MLIs are used expressively to solve power balancing issues [5], [6]. Since the integrated systems of renewable energy have comparatively lower efficiencies compared to conventional power systems, they require high voltage gains. The switched capacitor based MLIs satisfy this requirement because they can boost the voltage to a higher magnitude. It is worth mentioning that the switched capacitors can generate higher output voltage regardless of the supply voltage. Various switched capacitor based MLIs with voltage boost abilities are discussed in [7]–[10]. One

The associate editor coordinating the review of this manuscript and approving it for publication was Suman Maiti.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

of the topologies proposed switched capacitor units by sustaining a series/parallel connection with the DC-DC converter [8]. This DC-DC converter works as an inverter with an aid of an additional H-bridge device. It employs switching devices that require voltage ratings equal to the maximum voltage of the entire device and makes the MLI unsuitable for high voltage applications. Switched capacitor units based MLI also proposed [9]. Although this topology employs less number of power equipment where it requires an additional H-bridge circuit to generate the output voltage and thus leads to the higher total standing voltage of switches similar to the previous topology [8]. To resolve these issues, several MLI structures have been proposed [11]–[16]. For instance, one of the topologies has used four switched capacitors to produce nine-level voltage output [13]. However, two of these capacitors require voltage ratings which are twice of the input rating voltage and increases the overall cost of the system significantly. Three different topologies are also developed to generate seven-level output with a voltage gain factor of three [15]–[17]. However, the common drawback of these topologies is that they require a highe number of switching devices which increases the system cost, complexity and total standing voltage (TSV) of MLIs.

Although, switched capacitor based MLIs have lower TSV, they need higher power component counts to execute the capacitor voltage balancing operation and generate high voltage levels. To tackle this issue, asymmetric DC sources of unequal magnitudes topologies are considered which is decreases the number of switching devices [18]–[22]. Compared to the switched capacitor based MLIs, asymmetrical MLIs can generate higher voltage levels and it can be applied in medium and high voltage systems. In these MLI configurations, semiconductor devices are usually connected with different magnitude of DC sources. The switches that relate to the high magnitude of DC sources, generally experience high TSV. As a result, switches with high voltage ratings are required to be utilized. They are very costly. Furthermore, since these designs consist of the different magnitude of DC sources, they are not implemented in distributed power systems where the DC sources are required to symmetrical.

Considering all the pros and cons of the switched capacitor and asymmetrical based MLIs, this paper presents a novel configuration of MLI that can operate either by employing capacitors or only DC sources depending on the application requirement. The proposed topology does not require any extra H-bridge circuit to produce negative voltage levels which led to a significant reduction in TSV. Also, it does not require any complex control strategy or extra circuits to deal with voltage balancing, voltage ripples and high-power losses. It can be extended to produce higher voltage levels with two types of arrangements depending on the application requirements such as: (1) modularity and smart switching arrangements enables to produce different voltage levels utilizing more than one switching path. This provides higher flexibility and reliability in case of any malfunction in the power electric components; (2) it can function utilizing

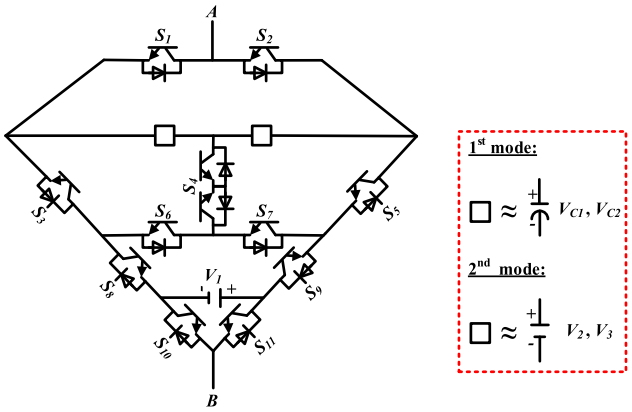


FIGURE 1. Schematic diagram of the proposed diamond-shaped multilevel inverter.

both symmetrical and asymmetrical DC sources. The module configuration of the proposed inverter including operating principle, mathematical explanations and module extension are discussed. A comparative study is carried out and their results are presented. The results are obtained from simulation and experiments are also presented and discussed.

II. PROPOSED DIAMOND SHAPED MULTILEVEL INVERTER

A. TOPOLOGY CONFIGURATION

The proposed diamond-shaped inverter has been illustrated in Fig. 1. It consists of ten unidirectional integrated bipolar transistors (IGBTs) such as S_1, S_2, S_3, S_5, S_6, S_7, S_8, S_9, S_{10} and S_{11} and one bidirectional IGBT i.e., S_4. During the switched capacitor mode (1st mode), it employs two switched capacitor (i.e., V_{C1} and V_{C2}) and one DC supply (V_1). It employs three DC sources (V_1, V_2 and V_3) of unequal magnitudes in the DC source mode (2nd mode). In the 1st mode of operation, the switching arrangements of the MLI allow the capacitors to connect in parallel with the DC source while charging and in series with the DC source while they discharge. The proposed MLI can generate 7-level output voltage such as $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm V_{DC}$ and 0 and 15-level output such as $\pm 7V_{DC}$, $\pm 6V_{DC}$, $\pm 5V_{DC}$, $\pm 4V_{DC}$, $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm V_{DC}$ and 0 for 1st and 2nd modes, respectively. The switching arrangement of the proposed MLI is selected in a way that the short-circuiting of the sources and capacitors can be avoided.

B. SWITCHING OPERATION OF 1ST MODE

The switching operation of the proposed MLI has been described for the positive half cycle. The operations are:

1) ZERO VOLTAGE LEVEL ($V_{AB} = 0$)

The voltage level is generated by turning 'on' S_2, S_5, S_9 and S_{11} switches. Also, S_4, S_6 and S_8 switches are turned 'on' to charge the capacitor V_{C2} in parallel with the DC supply V_{DC}. This switching arrangement will result in $V_{AB} = 0$ and $V_{C2} = +V_{DC}$. Capacitor V_{C1} is completely separated from the DC supply by keeping S_3 and S_7 switches 'off'.

TABLE 1. Switching states of 1st mode operation.

Switching sequences											Capacitor Supply Output			
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	V_{C1}	V_{C2}	V_1	V_{AB}
0	1	0	1	1	1	0	1	1	0	1	-	$+V_{DC}$	0	0
0	1	0	1	1	1	0	1	1	1	0	-	$+V_{DC}$	$+V_{DC}$	$+V_{DC}$
0	1	1	1	0	0	1	1	1	1	0	$+V_{DC}$	0	$+V_{DC}$	$+2V_{DC}$
0	1	1	0	0	1	1	0	1	1	0	0	0	$+V_{DC}$	$+3V_{DC}$
1	0	1	1	0	0	1	1	1	1	0	$+V_{DC}$	-	0	0
1	0	1	1	0	0	1	1	1	0	1	$+V_{DC}$	-	$-V_{DC}$	$-V_{DC}$
1	0	0	1	1	1	0	1	1	0	1	0	$+V_{DC}$	$-V_{DC}$	$-2V_{DC}$
1	0	0	0	1	1	1	1	0	0	1	0	0	$-V_{DC}$	$-3V_{DC}$

2) FIRST POSITIVE VOLTAGE LEVEL ($V_{AB} = +V_{DC}$)

This voltage level is generated by turning on S_2, S_5, S_9 and S_{10} switches. Like the earlier case, S_4, S_6 and S_8 are also remained at 'on' state to maintain the capacitor V_{C2} at charged state. In this case, the DC source is connected in series with the load V_{AB} and the output state will become $V_{AB} = +V_{DC}$. The state of capacitor V_{C1} will remain unchanged.

3) SECOND POSITIVE VOLTAGE LEVEL ($V_{AB} = +2V_{DC}$)

In this level, switches S_2, S_4, S_7, S_9 and S_{10} are utilized to connect the charged capacitor V_{C2} in series with the DC supply V_{DC} and used its stored energy. As a result, a voltage magnitude of $+2V_{DC}$ will appear across the load V_{AB}. Switches S_3 and S_6 are switched 'on' to connect and charge the capacitor V_{C1} in parallel with the DC source.

4) THIRD POSITIVE VOLTAGE LEVEL ($V_{AB} = +3V_{DC}$)

The proposed MLI produces the maximum voltage in this state by utilizing S_2, S_3, S_6, S_7, S_9 and S_{10} switches along with the energies stored in both capacitors. Result in an output voltage of $V_{AB} = +3V_{DC}$. After the completion of the positive cycle, the negative cycle will occur. In that instance, the charging and discharging state of the capacitors will be reversed. The charging and discharging times for both the capacitors are identical during the complete cycle of operation. It confirms that both capacitor voltages are balanced. For 1st mode, the switching sequence and operation of the diamond shaped MLI is demonstrated in Table 1 and Fig. 2, respectively.

The voltage stress of each switch is determined by observing the current paths as shown in Fig. 2. Since S_4, S_6, S_7, S_8, S_9, S_{10}, and S_{11} switches have the capability of blocking voltages and their magnitude like the DC supply voltage. While they are turned off, they all have voltage stress of V_{DC}. On the other hand, switches S_1, S_2, S_3, and S_5 have the capability of blocking voltages with a magnitude which is twice of the DC voltage supply. Thus, these four switches have voltage stress of $2V_{DC}$. Therefore, the TSV of the diamond shaped MLI is $16V_{DC}$. Fig. 3 illustrated the voltage stress under different switches.

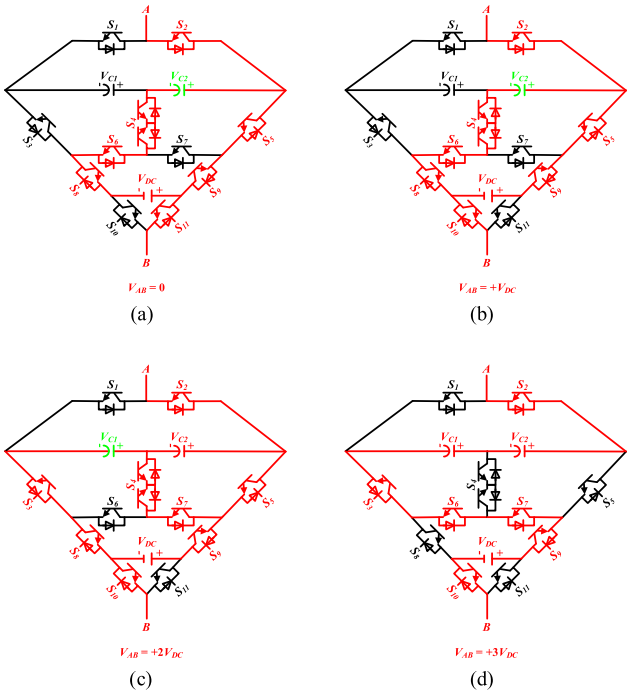


FIGURE 2. Switching operations and current paths of diamond shaped MLI for the positive cycle in 1st mode operation: (a) zero voltage, (b) 1st voltage level, (c) 2nd voltage level, (d) 3rd voltage level.

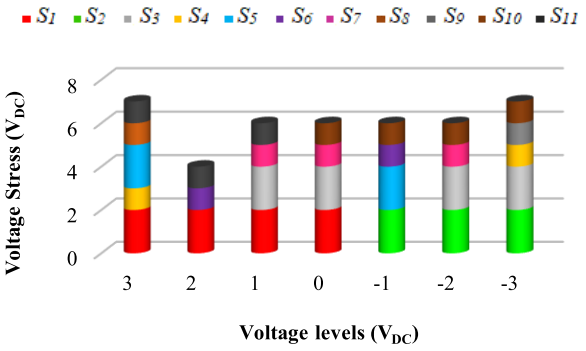


FIGURE 3. Voltage stress under different switches for 1st mode operation.

C. SWITCHING OPERATION OF 2ND MODE

In this operation, the diamond shaped MLI is constructed with 3DC sources of unequal magnitudes. The ratio between the top 2 DC sources (V_2, $V3$) and the bottom DC source (V_1) is 3:1. It is worth noting that the ratio is chosen in a way that the maximum output can be obtained. Also, the scale of the top DC sources is kept fixed at $3V_{DC}$ to ensure a balanced operation in both the negative and positive half cycle is maintained. The switching states of the diamond shaped inverter are presented in Table 2 along with the operation of the DC sources and the associated voltage steps for one full cycle.

The voltage stress of each switch can be determined similar to the 1st mode. Here, S_6, S_7, S_8, S_9, S_{10}, and S_{11} switches have the capability of blocking voltages having magnitude

TABLE 2. Switching states of 2nd mode operation.

Switching sequences											DC Sources			Output
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	V_1	V_2	V_3	V_{AB}
0	1	1	0	0	1	1	0	1	1	0	$+V_{DC}$	$+3V_{DC}$	$+3V_{DC}$	$+7V_{DC}$
0	1	1	0	0	0	0	1	0	1	0	0	$+3V_{DC}$	$+3V_{DC}$	$+6V_{DC}$
0	1	1	0	0	0	0	1	0	0	1	$-V_{DC}$	$+3V_{DC}$	$+3V_{DC}$	$+5V_{DC}$
0	1	0	1	0	0	1	0	1	1	0	$+V_{DC}$	0	$+3V_{DC}$	$+4V_{DC}$
0	1	0	1	0	0	1	0	1	0	1	0	0	$+3V_{DC}$	$+3V_{DC}$
0	1	0	1	0	1	0	1	0	0	1	$-V_{DC}$	0	$+3V_{DC}$	$+2V_{DC}$
0	1	0	0	1	0	0	0	1	1	0	$+V_{DC}$	0	0	$+V_{DC}$
0	1	0	0	1	0	0	0	1	0	1	0	0	0	0
1	0	1	0	0	0	0	1	0	0	1	$-V_{DC}$	0	0	$-V_{DC}$
1	0	0	1	0	0	1	0	1	1	0	$+V_{DC}$	$-3V_{DC}$	0	$-2V_{DC}$
1	0	0	1	0	0	1	0	1	0	1	0	$-3V_{DC}$	0	$-3V_{DC}$
1	0	0	1	0	1	0	1	0	0	1	$-V_{DC}$	$-3V_{DC}$	0	$-4V_{DC}$
1	0	0	0	1	0	0	0	1	1	0	$+V_{DC}$	$-3V_{DC}$	$-3V_{DC}$	$-5V_{DC}$
1	0	0	0	1	0	0	0	1	0	1	0	$-3V_{DC}$	$-3V_{DC}$	$-6V_{DC}$
1	0	0	0	1	1	1	1	0	0	1	$-V_{DC}$	$-3V_{DC}$	$-3V_{DC}$	$-7V_{DC}$

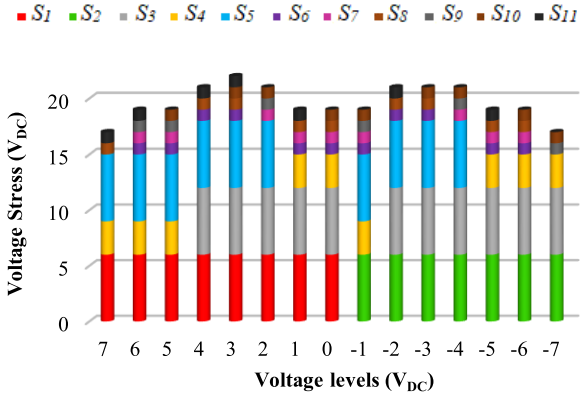


FIGURE 4. Voltage stress under different switches for 2nd mode operation.

similar to the voltage source V_1 while they are turned off. Therefore, they all have a voltage stress of V_{DC}. On the other hand, switches S_1, S_2, S_3, and S_5 have the capability of blocking voltages with a magnitude which is twice of the top DC sources (V_1 and V_2). Thus, these four switches have voltage stress of $6V_{DC}$. Finally, the bidirectional switch S_4 can block the $3V_{DC}$ voltage. Therefore, the TSV of the diamond shaped MLI is $33V_{DC}$. The voltage stress of each switch is shown in Fig. 4.

D. MODULARITY

The modularity of this diamond-shaped module is to generate higher voltage levels which is a noteworthy feature. The new MLI can be extended by connecting another unit (i.e., n^{th}) by utilizing a traditional cascaded assembly as shown in Fig. 5. The modularity of cascaded units is ensured by assuming that each module has the same number of power electric components. Thus, the proposed topology generates a high level of output voltage for both operation modes. The equations are used in this proposed diamond shaped MLI can be demonstrated in terms of voltage steps (N_L) generated by the MLI as follows.

1st mode operation

$$\text{Number of DC sources,} \quad N_{DC} = \frac{N_L - 1}{6} \tag{1}$$

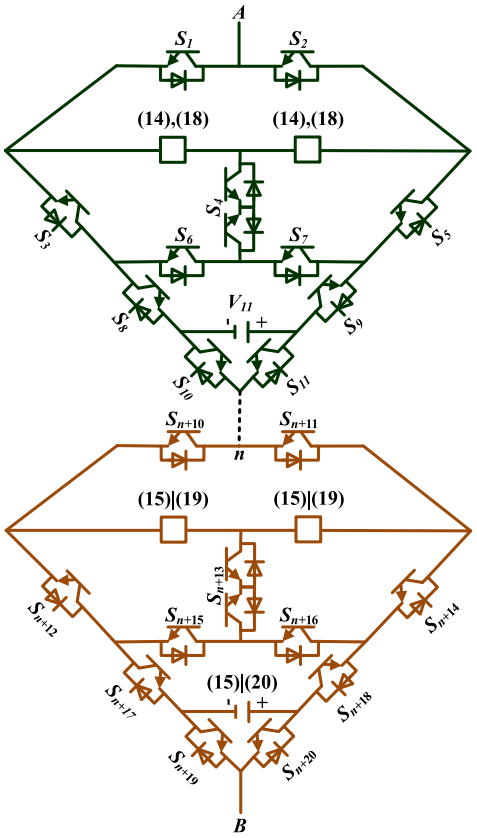


FIGURE 5. The modularity of the proposed diamond shaped MLI.

$$\text{Number of capacitors,} \quad N_C = \frac{N_L - 1}{3} \tag{2}$$

$$\text{Number of switches,} \quad N_S = 2\,(N_L - 1) \tag{3}$$

$$\text{Number of gate drivers,} \quad N_D = \frac{11(N_L - 1)}{6} \tag{4}$$

$$\text{Maximum voltage,} \quad N_{L\_max} = \frac{N_L - 1}{2} \tag{5}$$

$$\text{Variety of sources,} \quad N_{variety} = 1 \tag{6}$$

$$\text{TSV,} \quad N_{TSV} = \frac{8(N_L - 1)}{3} \tag{7}$$

2nd mode operation

$$\text{Number of DC sources,} \quad N_{DC} = \frac{3(N_L - 1)}{14} \tag{8}$$

$$\text{Number of switches,} \quad N_S = \frac{6(N_L - 1)}{7} \tag{9}$$

$$\text{Number of gate drivers,} \quad N_D = \frac{11(N_L - 1)}{14} \tag{10}$$

$$\text{Maximum voltage,} \quad N_{L\_max} = \frac{N_L - 1}{2} \tag{11}$$

$$\text{Variety of sources,} \quad N_{variety} = 2 \tag{12}$$

$$\text{TSV,} \quad N_{TSV} = \frac{8(N_L - 1)}{7} \tag{13}$$

E. VERSATILITY

The cascaded extension of the diamond shaped MLI can be established by choosing two different arrangements of the

units. These two arrangements explain the versatility of the proposed MLI. They are as follows.

1) 1ST ARRANGEMENT

The cascaded connection is established using n units of diamond shaped MLIs that are all operating at 1st mode operation. The equations regarding this arrangement are as follows.

Unit 1:

$$V_{C11} = V_{C12} = V_{11} = V_{DC} \tag{14}$$

Unit 2:

$$V_{C21} = V_{C22} = V_{21} = 3V_{DC} \tag{15}$$

From this arrangement, the total number n units of diamond shaped MLI can be determined as follows.

$$\left.\begin{array}{ll} N_L = 9n - 2, & \text{for odd } n \\ N_L = 12n + 1, & \text{for even } n \end{array}\right\} \tag{16}$$

$$N_{variety} = 2 \tag{17}$$

2) 2ND ARRANGEMENT

This arrangement is developed by combining n units of diamond shaped MLIs that are operating at two different modes. The magnitude of the 1st unit is the same as the 1st arrangement. The equations regarding this arrangement are as follows.

Unit 1:

$$V_{C11} = V_{C12} = V_{11} = V_{DC} \tag{18}$$

Unit 2:

$$V_{22} = V_{C23} = 3V_{DC} \tag{19}$$

$$V_{21} = V_{DC} \tag{20}$$

From this arrangement, the total number of n units of diamond shaped MLI can be determined as follows;

$$\left.\begin{array}{ll} N_L = 10n - 3, & \text{for odd } n \\ N_L = 10n + 1, & \text{for even } n \end{array}\right\} \tag{21}$$

$$N_{variety} = 2 \tag{22}$$

The above arrangements demonstrate the high versatility and flexibility in the power system applications of the proposed MLI. For instance, the 1st arrangement can be utilized in renewable energy integrated systems [23], motor drive control [24], electric vehicles [25], multilevel transceivers [26], transformer less UPS systems [27]. On the contrary, the 2nd arrangement can be applied where more than two capacitors can be avoided, for instance, in shunt active power filters (SAPF) [28], series filters (SEF) [29], static synchronous compensator (STATCOM) [3] and unified power quality conditioners (UPQC) [30].

F. POWER LOSS AND EFFICIENCY CALCULATION

The power loss and efficiency of the proposed MLI topology are determined by utilizing PLECS software. The power loss analysis is conducted in a steady-state condition with an ambient temperature of 25°C across all the heat sinks. It is ensuring that the heat is uniformly distributed across all the heat sinks. The thermal profiles of the IGBTs and the diodes are shown in Fig. 6. Here, E_{on_IGBT}, E_{off_IGBT} and E_{off_Diode} represents the turn 'on' energy losses of IGBTs, turn 'off' energy losses of IGBTs and turn 'off' energy losses of the diodes respectively. v_{drop_IGBT} and v_{drop_Diode} represent the forward voltage drops of the IGBTs and diodes while i_{on_IGBT} and i_{on_Diode} symbolize the current through the IGBTs and diodes respectively when they are operating. v_{on_IGBT} and v_{on_Diode} represent the 'on' state voltage of the IGBTs and diodes consecutively while they are conducting. The power loss characteristics of the IGBT switches and diodes are shown under two temperatures i.e., 25°C and 175°C in Fig. 6. The power loss for 1st and 2nd modes are determined at operating powers 900 W and 1.2 KW, respectively. The power loss of both modes of operation can be determined by as follows;

1) POWER LOSS IN 1ST MODE

The efficiency is determined by considering switching and conduction losses from IGBTs and diodes along with power losses from the switched capacitors. The power losses of the capacitors are calculated as follows:

$$P_C = P_D + P_R \tag{23}$$

$$P_D = (0.1u_{DC})^2 \times \pi \times f \times C \times \tan\delta_0 \tag{24}$$

$$P_R = I^2 R_S \tag{25}$$

where P_D and P_R are the dielectric and resistive losses, respectively and associated with the capacitors. Furthermore, u_{DC} is the maximum DC voltage applied to the capacitors, f is the fundamental frequency, C is the capacitance and $\tan\delta_0$ is the dissipation factor which is 0.15. The power loss associated with the capacitors is obtained 12.723W by solving equations (23) and (24). The total IGBT switching and conduction, diode switching and diode conduction losses are found 0.197 W, 9.374 W, 0.012 W and 0.889 W, respectively under the steady-state analysis. The efficiency of the MLI is 94.8% with a total power loss of 23.195 W.

2) POWER LOSS IN 2ND MODE

Since this mode does not require any switched capacitor units, the total power losses are calculated considering the switching and conduction losses of IGBTs and diodes. The total IGBT switching and conduction, diode switching and diode conduction losses are 0.959 W, 8.588 W, 0.009 W and 2.226 W, respectively under the steady-state analysis. The efficiency is calculated 97.7% with a total power loss of 11.782 W. Figure. 7 depicts the change of efficiency of the proposed MLI at different operating powers. It can be observed that the inverter has obtained its maximum

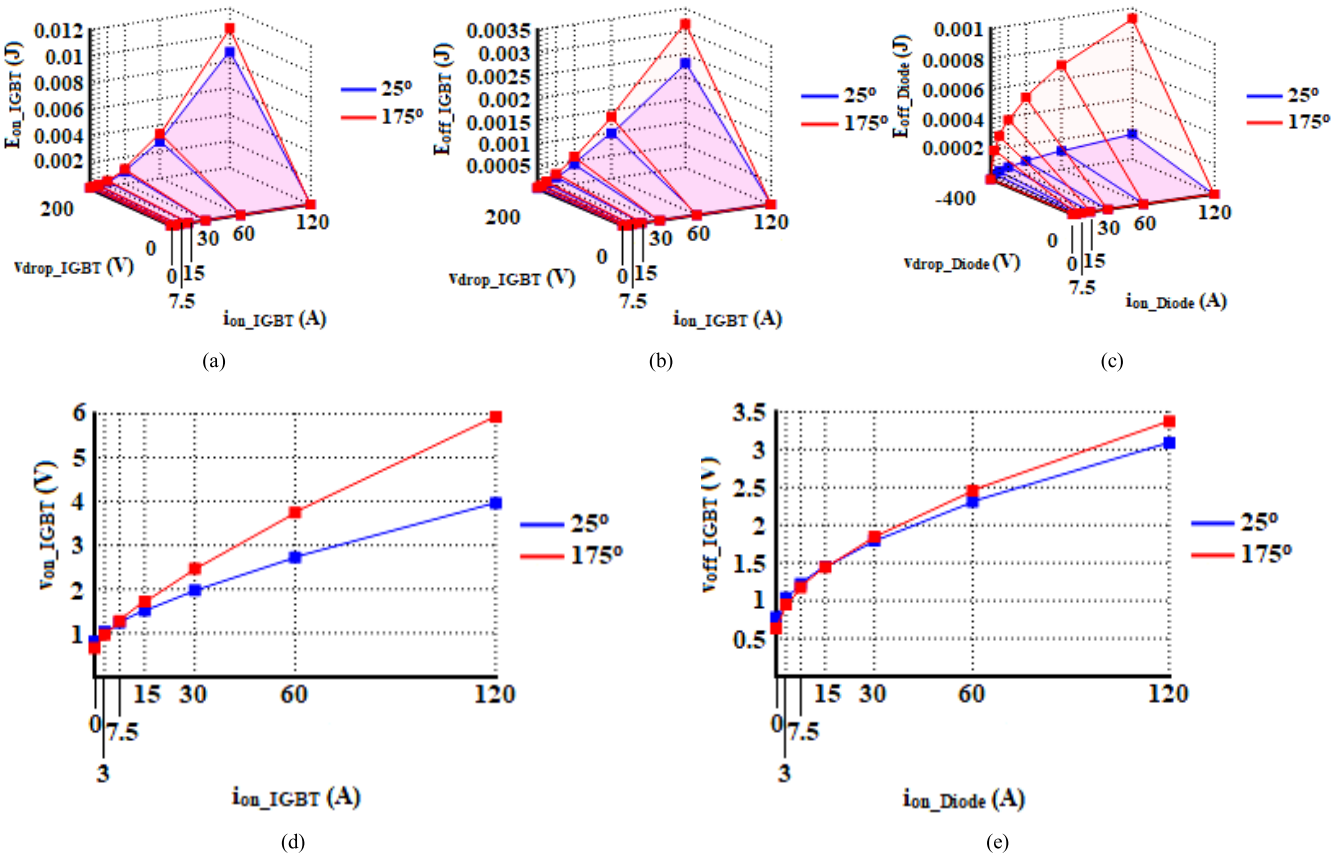


FIGURE 6. Thermal profile of: (a) IGBT turn-on losses, (b) IGBT turn-off losses, (c) diode turn-off losses, (d) IGBT conduction losses and (e) diode conduction losses.

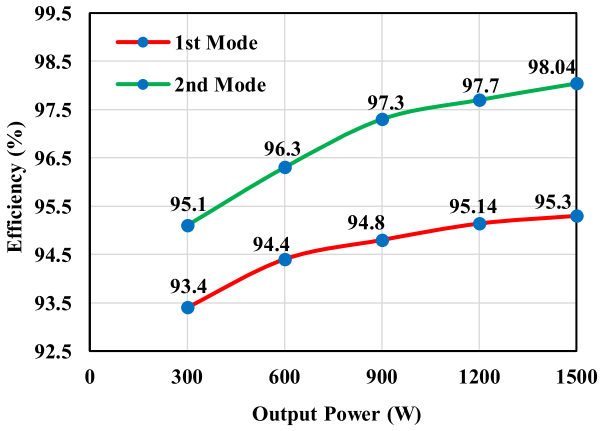


FIGURE 7. The efficiency of the diamond shaped MLI under different operating power.

efficiency of 95.3% and 98.04% for 1st and 2nd modes respectively while operating at 1.5 KW as shown in Fig. 7.

It can be observed that the steady-state losses for an MLI are almost same for all output power levels, so the efficiency at lower outputs (<10-15% of output power) is affected more. For higher operating power (>3.5 KW), this can be reversed as the MLI will be required IGBT devices with higher voltage ratings which will incur increased power losses.

G. CAPACITOR VOLTAGE RIPPLE ANALYSIS OF 1ST MODE

The total DC-link voltage to be constant to produce a high-quality AC output. Therefore, the voltage ripples created by switched capacitor units need to be small (i.e., <5%). The voltage ripples of both capacitors (C_1 and C_2) can be approximated by equation [9];

$$\Delta V_C = \frac{1}{\omega C} \int_{\theta_{on}}^{\theta_{off}} i_0 \, d\omega t \tag{26}$$

which can be further estimated by using fundamental output current of the diamond shaped MLI as follows;

$$\Delta V_C = \frac{I_{AB}}{\omega C} \int_{\theta_{on}}^{\theta_{off}} \sin(\omega t - \varphi) \, d\omega t \tag{27}$$

where ω is the fundamental angular frequency of the AC output voltage, φ is the angular displacement between voltage and current, θ_{off} is the end angle of voltage ripple while θ_{on} is the starting angle of voltage ripple and C is the capacitance of the capacitors. The ripple angles can be estimated by the following equations;

$$\theta_{on} = \sin^{-1}\left[\frac{N_{VR}+0.5}{Q \times m(N_C+1)}\right] \tag{28}$$

TABLE 3. Comparative analysis between MLIs (1st mode).

MLIs	N_S	N_D	N_G	N_C	N_{TSV}	N_T	Negative Levels
FC	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	N_L-1	$2(N_L-1)$	$7(N_L-1)$	Inherent
[8]	$5(N_L-1)/3$	$5(N_L-1)/3$	$5(N_L-1)/3$	$(N_L-1)/3$	$10(N_L-1)/3$	$16(N_L-1)/3$	H-bridge
[9]	$7(N_L-1)/3$	$7(N_L-1)/3$	$2(N_L-1)$	$(N_L-1)/3$	$4(N_L-1)$	$7(N_L-1)$	H-bridge
[10]	$13(N_L-1)/6$	$5(N_L-1)/3$	$13(N_L-1)/6$	$5(N_L-1)/6$	$3(N_L-1)$	$23(N_L-1)/3$	H-bridge
[13]	$7(N_L-1)/3$	$7(N_L-1)/3$	$7(N_L-1)/3$	$(N_L-1)/3$	$7(N_L-1)/3$	$22(N_L-1)/3$	Inherent
[14]	$7(N_L-1)/3$	$7(N_L-1)/3$	$7(N_L-1)/3$	$(N_L-1)/3$	$7(N_L-1)/3$	$22(N_L-1)/3$	Inherent
[15]	$7(N_L-1)/3$	$7(N_L-1)/3$	$2(N_L-1)$	$(N_L-1)/3$	$10(N_L-1)/3$	$7(N_L-1)$	Inherent
[16]	$8(N_L-1)/3$	$8(N_L-1)/3$	$7(N_L-1)/3$	$(N_L-1)/3$	$8(N_L-1)/3$	$8(N_L-1)$	Inherent
Diamond MLI (1st Mode)	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/3$	$8(N_L-1)/3$	$19(N_L-1)/3$	Inherent

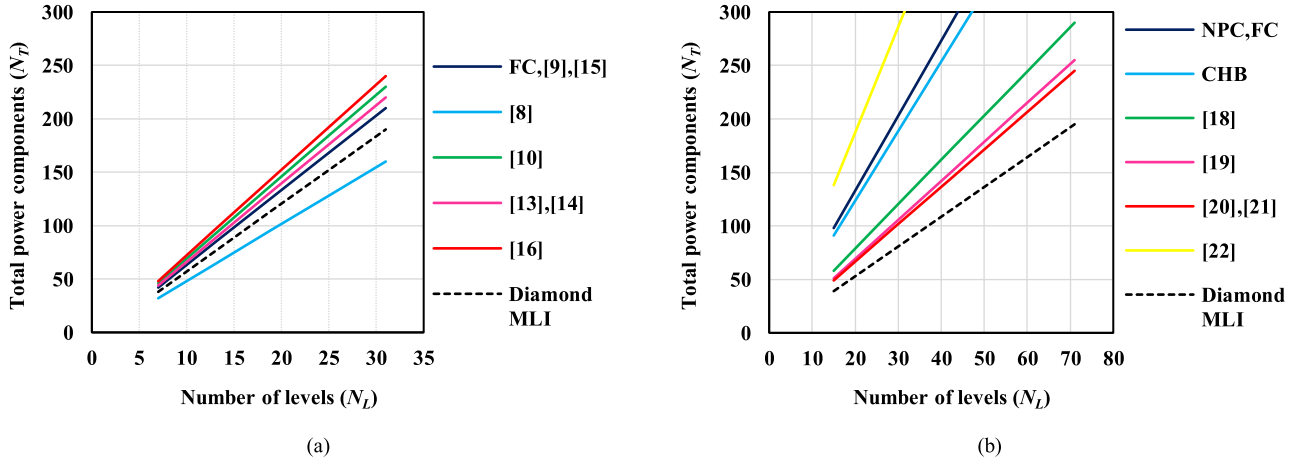


FIGURE 8. Comparison between MLIs in terms of total power components: (a) 1st mode, (b) 2nd mode.

$$\theta_{off} = \pi - \theta_{on} \tag{29}$$

where Q is the quality factor and m is the modulation index. N_{VR} is the specific voltage level for which the capacitor voltage ripple is calculated. Using equations (26) to (29), the capacitor voltage ripples for both capacitors are found 3.18 V. This indicates that the capacitor voltages have low ripples and can be utilized in the proposed MLI.

III. COMPARATIVE ANALYSIS

The predominance features of the proposed MLI is validated by comparing with recently developed MLI topologies. The comparisons are carried out in terms of the number of IGBT devices (N_S), diodes (N_D), gate drive circuits (N_{GDC}), capacitors (N_C), DC sources (N_{DC}), total standing voltage (N_{TSV}), total power components (N_T) and the requirement of additional H-bridge circuit.

A. COMPARISON OF 1ST MODE

The MLI topologies which have been utilized the switched capacitor units are only compared [8]–[16]. The detailed comparison in terms of power electric components is given in Table 3. Fig. 8(a) shows the comparison in terms of the total component. It can be stated that the proposed inverter requires a smaller number of active switches and gate driver circuits compared to other MLIs except for the topology proposed in [8]. Although this topology required a smaller number of IGBTs, it has a higher amount of TSV compared to other MLIs [13]–[16] due to an additional H-bridge circuit that has been utilized by the MLI to produce negative levels. In fact, it can be observed that the other topologies [8]–[10] require a backend H-bridge circuit and they are comparatively higher TSV than the MLIs that do not require. It possesses a significant disadvantage for these MLIs as the higher TSV can decrease their efficiency and question the reliability of their performances in industrial uses. Furthermore, two topologies proposed in [13], [14] provide slightly lower TSV compared to the diamond shaped MLI. However, both MLIs require a higher number of semiconductor devices and gate driver circuits which can increase the manufacturing cost of the MLIs.

The topology which is similar to the diamond shaped MLI in terms of power electric components is proposed in [10]. It even requires a smaller number of diodes compared to diamond shaped MLI. Nevertheless, this MLI has also significant disadvantages such as; it requires 3 flying capacitors which can cause capacitor voltage balancing issues and it also requires a superfluous H-bridge circuit which has contributed to its higher TSV.

TABLE 4. Comparative analysis between MLIs (2nd mode).

MLIs	N_S	N_D	N_G	N_{DC}	N_{TSV}	N_T	Negative Levels
NPC	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	N_L-1	$2(N_L-1)$	$7(N_L-1)$	Inherent
FC	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	N_L-1	$2(N_L-1)$	$7(N_L-1)$	Inherent
CHB	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$	$2(N_L-1)$	$13(N_L-1)/2$	H-bridge
[18]	$(N_L+5)/2$	$2(N_L-1)$	$(N_L+5)/2$	$(N_L+5)/2$	$(9N_L-39)/2$	$(7N_L+11)/2$	Inherent
[19]	$(N_L+7)/2$	$2(N_L-4)$	$(N_L+7)/2$	$(N_L-1)/2$	$5(N_L-1)/2$	$(7N_L-3)/2$	Inherent
[20]	N_L+1	N_L+1	N_L+1	$(N_L-1)/2$	$35(N_L-1)/7$	$7(N_L-1)/2$	Inherent
[21]	N_L+1	N_L+1	N_L+1	$(N_L-1)/2$	$2(N_L-1)$	$7(N_L-1)/2$	H-bridge
[22]	$2N_L$	$2N_L$	$2N_L$	$7(N_L-9)/2$	$3(N_L-1)$	$(19N_L-9)/2$	H-bridge
Diamond MLI (2nd Mode)	$6(N_L-1)/7$	$6(N_L-1)/7$	$2(N_L-1)$	$3(N_L-1)/14$	$33(N_L-1)/14$	$39(N_L-1)/14$	Inherent

B. COMPARISON OF 2ND MODE

In this case, the number of capacitors is replaced by the number of DC sources. The comparative results are presented in Table 4 and Fig. 8(b). It can be observed that the proposed MLI requires a smaller number of switches compared to other MLIs except for the MLIs proposed in [18], [19]. However, both MLIs require a higher number of diodes that ultimately increase the total equipment counts as shown in Table 4. Furthermore, they have higher TSV compared to the proposed module which can be problematic in case of higher power applications. Comparing the TSV parameters it can be noticed that the conventional MLIs along with the MLI proposed in [21] has lower TSV than the proposed MLI operating at 2nd mode. However, these MLIs have their shortcomings. For instance, the NPC and FC inverters have voltage balancing issues that result in higher complexities if the high voltage level is required. Multicell CHB inverters also consist of voltage balancing issues especially in distributed solar PV systems as reported by [31]. In the case of [21], it requires a higher number of power electric components which further added complexity in terms of closed-loop control and PWM techniques. Recently developed MLIs [11], [12], [33]–[35] utilized a low number of power electric components compared to the proposed topology. However, none of these MLIs could operate in dual mode since they require additional voltage balancing circuits to operate in switched capacitor mode.

Finally, it can be summarized that the most advantageous features of the switched capacitor based MLIs are (1) lower TSV compared to the asymmetric DC source-based topologies, (2) malfunction of switching devices can be easily fixed because the switches have similar voltage ratings, (3) cost-efficient to build and no voltage regulation is required since they generally operate utilizing a single DC source. On the contrary, the asymmetric MLIs have benefits such as it can produce a higher number of voltage levels utilizing a low number of components. The controls of these MLIs are very simple as they do not require voltage balancing also highly efficient as do not produce capacitor losses. It can also produce high-quality voltage output since there are no capacitor-based voltage ripples which will eventually enable them to reduce the total harmonic distortions (THD) significantly. It can be concluded that both modes of operations have their fair share of advantages and disadvantages.

C. COMPARISON BETWEEN 1ST MODE AND 2ND MODE IN TERMS OF RENEWABLE ENERGY APPLICATIONS

In renewable energy applications, the 1 st mode of operation is more superior and suitable than the 2nd mode. This statement can be validated by taking two applications into consideration which are: a distributed maximum power point tracker (MPPT) integrated MLI system [31] and a fuel cell integrated MLI system [32]. In the distributed system, the implemented MLI should resolve the power balancing issues such as voltage balance/phase and voltage balance/cell. In this application, the 2nd mode can create problems since it comprises of DC sources of two different magnitudes. The MPPTs connected with these DC sources require to have individual control scheme so that it can maintain the voltage. In addition, the high magnitude DC sources (V_2, V_3) of the 2nd mode of diamond MLI needs to have voltage which is exactly 3 times of the voltage of the low magnitude DC source (V_1) to maintain the 3:1 ratio otherwise, the entire MLI system would fail. Since it is a well-known fact that PV systems are highly intermittent and cause serious voltage fluctuations. Hence, there is a high chance that the 2nd mode will not be suitable for this application. Whereas the 1st mode can easily be implemented for the distributed system because it only comprises of a single DC source which is utilized conventional CHB MLI. The 1st mode improves the structure of the distributed system proposed in [31]. Since, it can generate the same number of voltage levels by utilizing only a single cell of MLI which is opposed to 3 CHB cells of the proposed system. Therefore, per cell voltage imbalance can be avoided without implementing any separate control scheme.

The fuel cell integrated system utilized 2 CHB MLIs and dual control mechanism to control two grid systems integrated with a single fuel cell. The implementation of 2nd mode configuration would be difficult since higher magnitude DC sources required a separate filter and transformer which can increase the overall cost of the system significantly. Furthermore, as the system has implemented two symmetrical CHB MLIs, it will be easier to implement the dual

control mechanism with a similar set of control parameters. However, CHB MLIs have issues such as high TSV, low efficiency and high component count. In this regard, the 1st mode of diamond MLI has the potential to replace CHB MLI by introducing beneficial features such as higher voltage levels, higher efficiency, lower THD, lower switching stress and overall performance enhancement.

D. COMPARISON WITH SIMILAR MLI STRUCTURES

In literature, various MLI configurations are available which is similar to the proposed configuration. Hence, it is highly important to compare those MLI topologies with the proposed configuration in order to further justify the main objective of this manuscript. The MLI proposed in [33] utilized 12 switches to produce 19-level output voltage. However, it consists of an H-bridge circuit which has contributed to higher voltage stress. It also comprises of two transformers to maintain 1:2 voltage ratio between the upper H-bridge circuit and the lower circuit. Therefore, the overall cost of this topology is higher compared to the proposed diamond shaped MLI. Furthermore, this MLI would not be suitable either for the distributed MPPT system or the fuel cell integrated grid system since the transformers utilized in this topology require individual voltage balancing mechanisms. Another MLI topology proposed in [34] also consists of 12 switches and it can generate 13-level output voltage. Since this MLI is build following symmetrical configuration like the proposed MLI, it can be applied in both distributed MPPT system and the fuel cell integrated MLI system. However, it contains a backend H-bridge circuit and 6 switched capacitors. The backend H-bridge circuit woul significantly increase the total voltage stress of the topology whereas the extra capacitors would contribute to high capacitor losses in the system and may heavily decrease the overall efficiency of the MLI. A topology named square T-type MLI (ASTMLI) proposed in [35] has utilized 12 switches to produce 17-level output voltage. Even though it is capable of producing an impressive number of voltage levels, it comprises of asymmetrical DC sources which limit its application in renewable energy systems as discussed earlier.

IV. SIMULATION RESULTS AND DISCUSSION

The function and performance of the proposed diamond shaped MLI are validated by simulation. The model is operated at an output power of 900 W while operating at 1st mode of operation whereas it is operated at 1.2 KW during the 2nd mode of operation. Table 5 illustrated the simulation parameters and hardware specifications of the diamond shaped MLI. The gate pulses of the proposed module are generated using a level shifted SPWM technique [35]. The method utilized in this study follows a carrier wave arrangement where all the carrier waves above the zero reference are in phase but opposite with those below zero references. Since this module can synthesize $N_L = 7$ and $N_L = 15$ voltage levels respectively for 1st and 2nd modes of operation, it will require 6 and 14 carrier waves and each of having a frequency of f_{cr} and an amplitude of A_{cr}. The equations related to SPWM technique are shown in (30) and (31).

TABLE 5. Simulation parameters and hardware specifications of the diamond shaped MLI.

Parameters	Symbol		Value/Model	
	1st mode	2nd mode	1st mode	2nd mode
DC source voltage	V_1	V_1, $V_2 - V_3$	100 V	50 V, 150 V
AC output voltage	V_{AB}		300 V	350 V
AC output current	I_{AB}		3 A	3.5 A
Resistive-inductive load	AB		100Ω-0.01H/253Ω-0.53H	
Fundamental frequency	f		50 Hz	
Switching frequency	f_{sw} | f_{cr}		2.5 kHz/5 kHz	
Semiconductor devices	$S_1 - S_{11}$		IGB30H60H3 (30 A and 600 V)	
Capacitors	C_1 and C_2		ESMQ201VSN272MA50S (2700 µF and 200 V)	
Gate driver optocoupler	-		HCPL3120	
Gate driver IC	-		SN7411C04N	

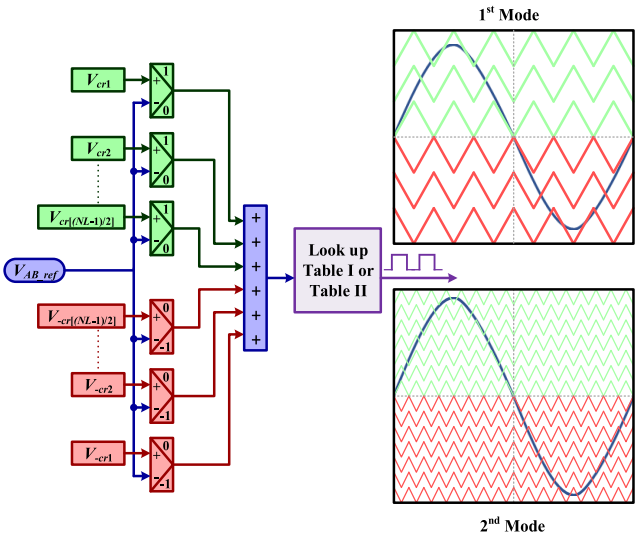


FIGURE 9. The control diagram of SPWM and carrier wave generation.

$$m_f = \frac{f_{cr}}{f} \tag{30}$$

$$m = \frac{A_m}{A_{cr} \times \dfrac{N_L - 1}{2}} \tag{31}$$

Here, m_f is the frequency modulation index, m represents the amplitude modulation index and A_m is the amplitude of the modulating signal (V_{AB_ref}). The control diagram of SPWM technique along with the generation of a carrier wave is shown in Fig. 9. To execute this technique, the carrier signals above the zero reference and the carriers below the zero reference are identified initially. At all moment, every single carrier wave is contrasted with the reference signal. In case of positive carriers, if the carrier waves are less than the reference signal then the comparison will give '1' as output and '0' otherwise. On the contrary, for the negative carriers, if the they are greater than the reference wave then the comparison will generate '−1' as output and '0' otherwise.

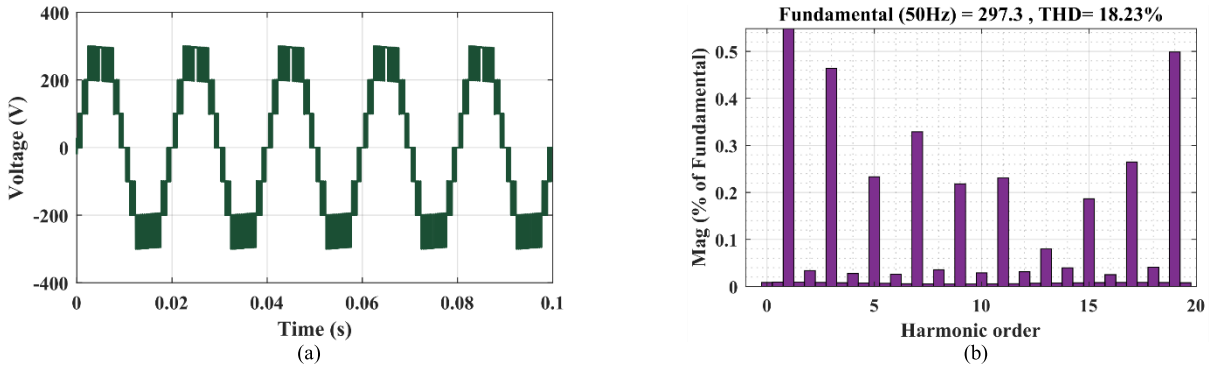


FIGURE 10. Simulation results of diamond-shaped MLI at 1st mode: (a) 7-level output voltage, (b) harmonic spectrum.

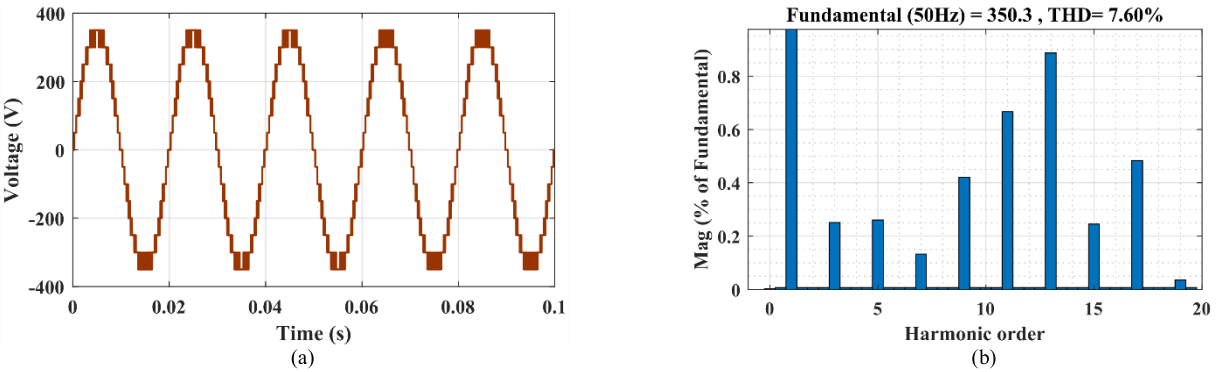


FIGURE 11. Simulation results of diamond-shaped MLI at 2nd mode: (a) 15-level output voltage, (b) harmonic spectrum.

The pulses acquired from these evaluations are then mathematically summed to obtain the switching states. Finally, gate pulses are derived by comparing these switching states with the switching sequences of the proposed MLI shown in Table 1 and Table 2 . These gate Pulses are further applied in the switches of the inverter to generate the simulation outputs.

Fig. 9(a) and Fig. 10(a) illustrate the output voltages of the novel diamond shaped MLI operating at 1st and 2nd modes, respectively. On the other hand, the harmonic spectrums are shown in Figure. 10(b) and Figure. 11(b). It can be noticed that the proposed MLI has produced higher total harmonic distortions (THD) while operating at 1st mode compared to the 2nd mode. Two main reasons can be identified behind these shortcomings. They are (1) low level of output voltage and (2) capacitor voltage ripples. Besides, the output voltage quality is also better for the 2nd mode compared to 1st mode. The issue of higher THD can be eliminated either by applying another modulation technique named selective harmonic elimination (SHE) or increasing the number of voltage levels by following one of the arrangements as described in section II. However, it should be noted that eliminating THD is not an objective of this manuscript.

The proposed inverter's performance has been verified in this section by integrating it with a PV system using MATLAB Simulink. It has also justifed the MLI's application that was highlighted in section 3.

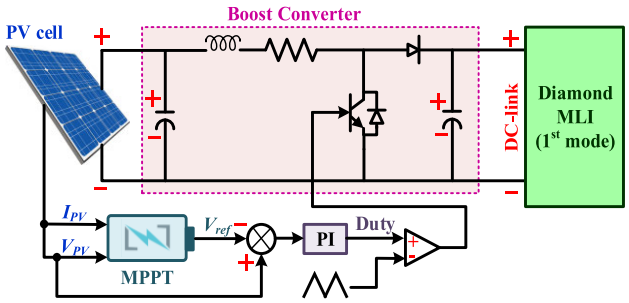


FIGURE 12. PV integration with the diamond shaped MLI.

V. PV INTEGRATION AND PERFORMANCE ANALYSIS

The diamond shaped MLI is integrated with a 100 KW PV system to analyze its performance in high power system using MATLAB Simulink. The PV cell's maximum power is regulated by using perturb and observe (P & O) based MPPT. Furthermore, a close loop controlled conventional boost converter is added to regulate and boosting the PV voltage. The capaticance and the inductance of the boost converter is calculated using the information provided in []. The paramteres involving the PV system as well as the boost converter are demonstrated in Table 6. The complete architecture of the system is illustrated in Fig 12.

The performance of the diamond shaped MLI (1st mode) is observed under varying irradiance of the solar cell from

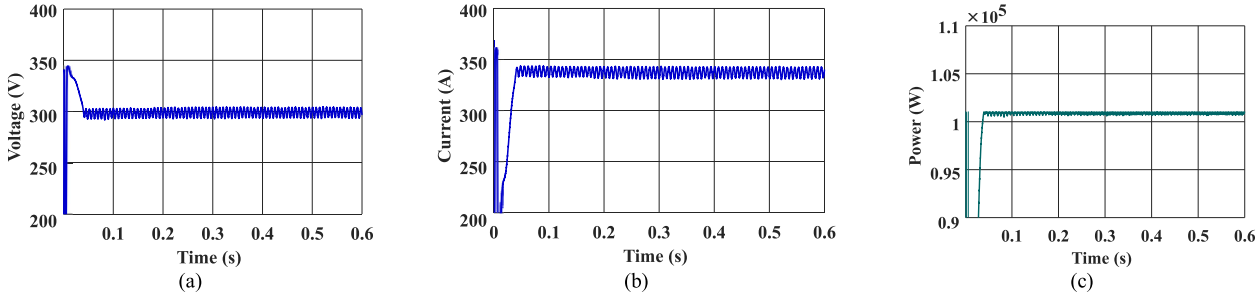


FIGURE 13. Simulation results of PV module: (a) output voltage, (b) output current, (c) rated power.

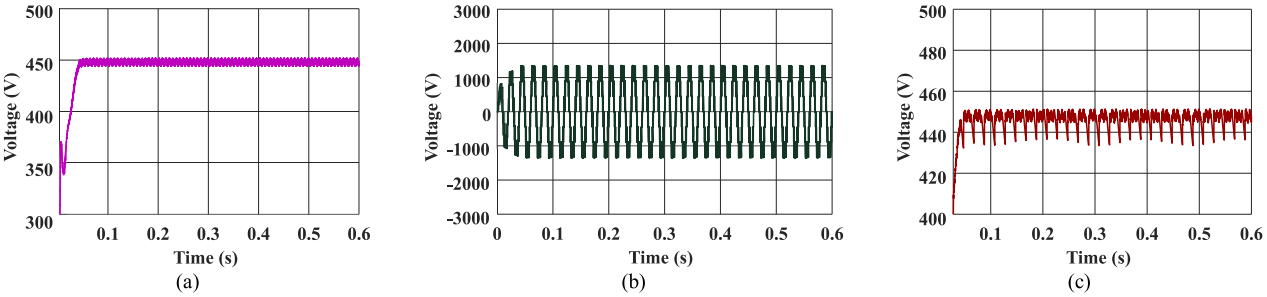


FIGURE 14. Simulation results of PV integrated diamond MLI: (a) DC-link voltage, (b) output voltage, (c) capacitor voltage.

TABLE 6. PV system parameters.

Parameters	Value
Parallel strings	47
Series connected modules	5
Open circuit voltage	360 V
PV voltage	300 V
PV current	335 A
Rated Power	100 KW
Switching frequency (boost converter)	5 KHz
Capacitance (boost converter)	327 μF
Inductance (boost converter)	1.43 mH
DC-link (boost converter)	450 V
Output voltage (inverter)	1350 V
Capacitor voltage drop (inverter)	1.11 %

1000 w/m^2 to 700 w/m^2 at 0.3 sec. The results of the PV system including the voltage, current and power are shown in Fig. 13(a), Fig. 13(b), and Fig 13(c). respectively. It can be observed from Fig. 14(a) that even after changing the irradiance the DC-link voltage has remained stable because of MPPT and the boost converter. It should be noted that since the 1st mode of diamond shaped MLI incorporates only one DC source, a single boost converter is enough to stabilize the voltage. However, MLIs having more than one DC source would require multiple converters or voltage oriented controllers [30]. In Fig. 14(b) the seven level ouput voltage (1350 V) of the proposed MLI is shown where no distortions can be observed during the change of irradiance at 0.3 sec. It also indicates accurate performance of the MLI. Furthermore, the capacitor voltage is shown in Fig. 14 (c). The maximum voltage drop of only 15 V (1.11 %) can be

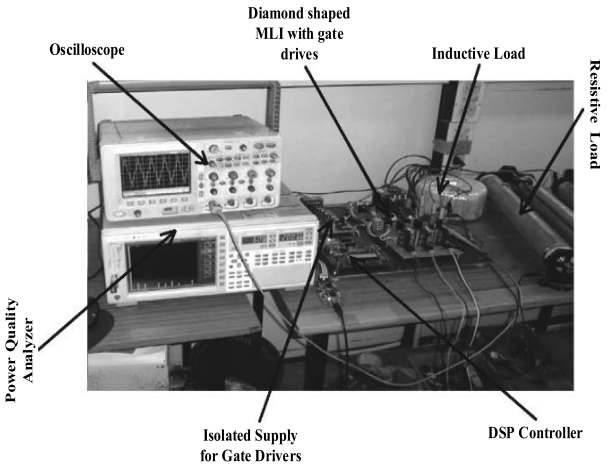


FIGURE 15. Hardware prototype of the diamond shaped MLI.

observed during the change of irradiance at 0.3 sec. Nevertheless, this voltgae drop is less than 5% (<67.5 V) of the total output voltage of the inverter. Thus, the voltage drop across the capacitor followed the National Electrical Code Standard (NEC 210-19 FPN No.4).

VI. EXPERIMENTAL RESULTS AND DISCUSSION

The outputs and performance of the proposed MLI are further validated by building a hardware prototype using TMS320F28335 digital signal processor (DSP). Three types of performance variations are carried out for both operating modes. The variations are: (i) the modulation index, (ii) the switching frequency and (iii) the loads or power factor (pf).

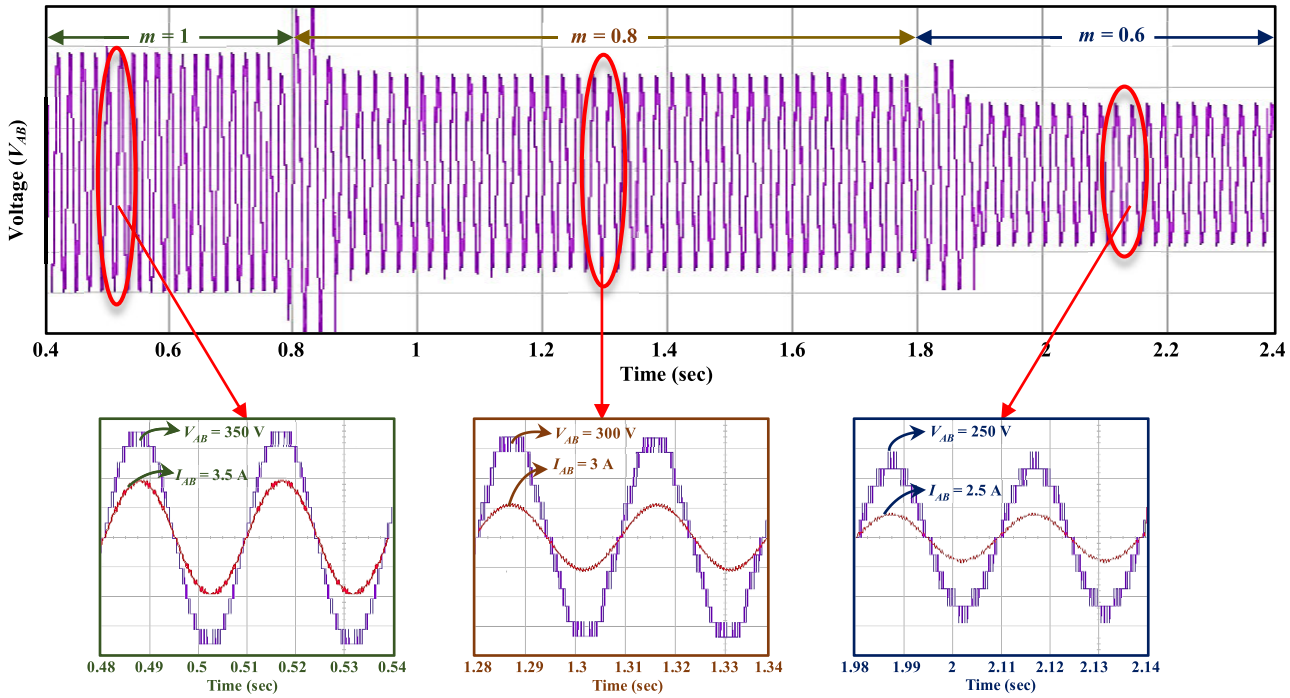


FIGURE 16. Transient performance analysis of diamond shaped MLI under variable modulation index.

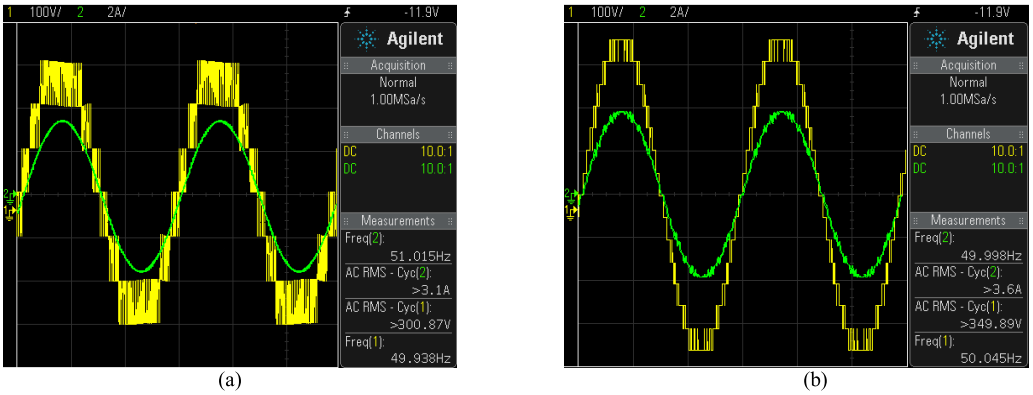
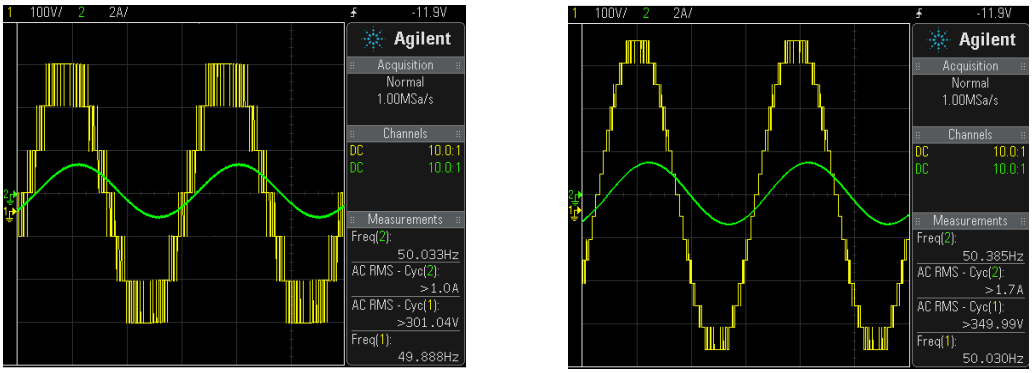


FIGURE 17. Experimental results of output voltage (yellow) and current (green) at f_{sw} = 5 kHz: (a) 1st mode, (b) 2nd mode.

The hardware prototype of the proposed diamond shaped MLI is shown in Fig. 15.

Fig. 16 illustrates the output voltage (V_{AB}) for 2nd modes of operation under variation of modulation index. This transitional performance analysis was achieved by integrating the diamond shaped MLI with a single phase induction motor while operating at 2nd mode. The speed of the motor is regulated by implementing v/f control as proposed in [24]. By changing the reference synchrnous speed of the motor, the output voltage of the inverter is observed. The motor is operated at three different speeds; 1500 rpm, 1200 rpm (at 0.8 sec) and 900 rpm (at 1.8 sec). Thus, the modulation index were changed from $m = 1$ to $m = 0.8$ at 0.4 sec while $m = 0.8$ to $m = 0.5$ at 0.8 sec. In these transitions, the output voltage of the proposed MLI changed from 350 V $\rightarrow$ 300 V $\rightarrow$ 250 V while at the same time the output voltage levels changed from 15 $\rightarrow$ 13 $\rightarrow$ 11. It can be observed that the proposed MLI performed well in all three transitions without any error. In this case study, the power factor (pf) was considered to be 1 and the switching frequency was 2.5 kHz.

Fig. 17(a) and Fig. 17(b) illustrate the output voltage for 1st and 2nd modes of operation respectively where the switching frequency increases to $f_{sw} = 5$ kHz. At both cases, the pf = 1 and the modulation index is $m = 1$. For the 1st mode, the MLI has generated the usual 7-level voltage output (300 V) with the output current of 3.1 A whereas, in the 2nd mode it synthesized 15-level voltage output (350 V) with the output current of 3.6 A. These results suggest that



(a) (b)

FIGURE 18. Experimental results of output voltage (yellow) and current (green) at pf = 0.8: (a) 1st mode, (b) 2nd mode.

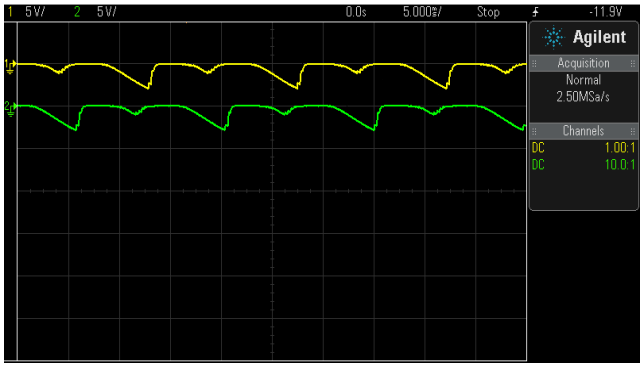


FIGURE 19. Experimental results of capacitor voltages for 1st mode.

the proposed MLI can operate at higher switching frequency accurately.

Fig. 18(a) and Fig. 18(b) illustrate the output voltage for 1st and 2nd modes of operation respectively where the single-phase resistive load is changed to $257\Omega - 0.53\text{H}$ and as well as the power factor to pf $= 0.8$. The modulation index and the switching frequency were set to $m = 1$ and $f_{sw} = 2.5$ kHz respectively for both modes of operation. For both modes of operation, it can be observed that the voltage level remained the same, but the current is decreased. In the 1st mode, the current decreased from 3.1A to 1.0A whereas, in the 2nd mode, the current decreased from 3.6A to 1.7A. However, in both cases no external distortions, noise or voltage instability can be observed. This indicates that the proposed MLI is operating without any issues when the power factor is altered. Finally, in Fig. 19 the capacitor voltages during the 1st mode of operation are illustrated. The voltage of 1st capacitor V_{C1} is depicted by yellow color whereas, the voltage of 2nd capacitor V_{C2} is depicted by green color. It can be concluded that both capacitor voltages are stable at 100 V with a low voltage ripple of 3.18%.

VII. CONCLUSION

The objective of the paper was to introduce a novel diamond shaped multilevel inverter. The proposed MLI topology can be employed in both switched capacitor units and DC voltage sources having dual-mode characteristics. The major contribution of this manuscript can be realized from the comparative analysis done between the proposed MLI and other recently developed MLIs. The detailed analysis has showcased the the advantages of the proposed MLI topology. configuration. Some noteworthy advantages are: it reduced the voltage stress on the switches due to the absence of a backend H-bridge circuit, it can generate higher voltage level utilizing reduced switch count, and it can be extended using two types of arrangements depending on the application requirements. These features made the proposed topology more efficient and economical as compared to the other MLIs.

Some noteworthy advantages are: it reduced the voltage stress on the switches due to the absence of a backend H-bridge circuit, it can generate higher voltage level utilizing reduced switch count, and it can be extended using two types of arrangements depending on the application requirements. These features made the proposed topology more efficient and economical as compared to the other MLIs.

The advantages of the diamond shaped MLI compared to other MLIs having similar attributes are also highlighted in terms of renewable energy applications. It was also identified that the 2nd mode of operation have some applications based limitations due to utilizing different magnitude of DC sources. This limitation has made this topology an interesting candidate for future analysis and improvement.

The simulation results were verified by developing an experimental prototype of the proposed MLI and testing it under dynamic load variation, different modulation indices and different switching frequencies without changing any functionalities regarding its power components. The results were highly satisfactory and hence, it can be concluded that the proposed module can be a leading candidate for a power electronic device in various industrial applications.

CONFLICTS OF INTEREST

The authors declare no conflict of interest.

REFERENCES

[1] S. T. Meraj, N. Z. Yahaya, K. Hasan, and A. Masaoud, "Single phase 21 level hybrid multilevel inverter with reduced power components employing low frequency modulation technique," *Int. J. Power Electron. Drive Syst.*, vol. 11, no. 2, pp. 810–822, 2020.
[2] M. K. Hasan, A. A. Habib, S. Islam, A. T. A. Ghani, and E. Hossain, "Resonant energy carrier base active charge-balancing algorithm," *Electronics*, vol. 9, no. 12, p. 2166, Dec. 2020.
[3] K. H. Law, "An effective voltage controller for quasi-Z-source inverter-based STATCOM with constant DC-link voltage," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8137–8150, Sep. 2018.
[4] D. Ahmadi and J. Wang, "Online selective harmonic compensation and power generation with distributed energy resources," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3738–3747, Jul. 2014.
[5] S. Essakiappan, H. S. Krishnamoorthy, P. Enjeti, R. S. Balog, and S. Ahmed, "Multilevel medium-frequency link inverter for utility scale photovoltaic integration," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3674–3684, Jul. 2015.
[6] P. Kala and S. Arora, "A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications," *Renew. Sustain. Energy Rev.*, vol. 76, pp. 905–931, Sep. 2017.
[7] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Mar. 2014.
[8] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.
[9] A. Taghvaie, A. Alijani, M. E. Adabi, M. Rezanejad, J. Adabi, K. Rouzbehi, and E. Pouresmaeil, "An asymmetrical step-up multilevel inverter based on switched-capacitor network," *Sustainability*, vol. 11, no. 12, p. 3453, Jun. 2019.
[10] H. K. Jahan, M. Abapour, and K. Zare, "Switched-capacitor-based single-source cascaded H-bridge multilevel inverter featuring boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1113–1124, Feb. 2019.
[11] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-type) module: Asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7148–7156, Nov. 2016.
[12] S. T. Meraj, K. Hasan, and A. Masaoud, "A novel configuration of cross-switched T-type (CT-type) multilevel inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3688–3696, Apr. 2020.
[13] X.-J. Ge, Y. Sun, Z.-H. Wang, and C.-S. Tang, "A single-source switched-capacitor multilevel inverter for magnetic coupling wireless power transfer systems," *Electr. Eng.*, vol. 101, no. 4, pp. 1083–1094, Dec. 2019.
[14] Y. C. Fong, S. R. Raman, M. M. Chen, and K. W. E. Cheng, "A novel switched-capacitor multilevel inverter offering modularity in design," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018, pp. 1635–1640.
[15] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.
[16] S. S. Lee, "A single-phase single-source 7-level inverter with triple voltage boosting gain," *IEEE Access*, vol. 6, pp. 30005–30011, 2018.
[17] A. K. M. A. Habib, S. M. A. Motakabber, M. I. Ibrahimy, and M. K. Hasan, "Active voltage balancing circuit using single switched-capacitor and series LC resonant energy carrier," *Electron. Lett.*, vol. 56, no. 20, pp. 1036–1039, Sep. 2020.
[18] R. Raushan, B. Mahato, and K. C. Jana, "Comprehensive analysis of a novel three-phase multilevel inverter with minimum number of switches," *IET Power Electron.*, vol. 9, no. 8, pp. 1600–1607, Jun. 2016.
[19] B. Mahato, S. Mittal, S. Majumdar, K. C. Jana, and P. K. Nayak, "Multilevel inverter with optimal reduction of power semi-conductor switches," *Renew. Energy Innov. Technol.*, pp. 31–50, 2018.
[20] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched DC sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, Jul. 2014.
[21] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Extended multilevel converters: An attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters," *IET Power Electron.*, vol. 7, no. 1, pp. 157–166, Jan. 2014.
[22] V. Nair R, A. Rahul S, R. S. Kaarthik, A. Kshirsagar, and K. Gopakumar, "Generation of higher number of voltage levels by stacking inverters of lower multilevel structures with low voltage devices for drives," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 52–59, Jan. 2017.
[23] F. L. Luo and H. Ye, "Switched-capacitor multilevel DC/AC inverters in solar panel energy systems," *Adv. DC/AC Inverters*, pp. 243–252, 2017.
[24] S. T. Meraj, K. Hasan, and A. Masaoud, "Design and application of SPWM based 21-level hybrid inverter for induction motor drive," *Turkish J. Electr. Eng. Comput. Sci.*, vol. 28, no. 6, pp. 3219–3234, 2020.
[25] A. K. M. A. Habib, M. K. Hasan, M. Mahmud, S. M. A. Motakabber, M. I. Ibrahimya, and S. Islam, "A review: Energy storage system and balancing circuits for electric vehicle application," *IET Power Electron.*, vol. 14, no. 1, pp. 1–13, Jan. 2021.
[26] K. Kumar, B. Pandey, D. M. A. Hussian, A. Bhutto, A. K. Pandit, and Y. A. B. El-Ebiary, "Design of multilevel modelling transceiver on spartan-3 and spartan-6 FPGA," *Int. J. Innov. Technol. Exploring Eng.*, vol. 8, no. 12s2, pp. 23–26, 2019.
[27] L. G. Fernandes, A. A. Badin, D. F. Cortez, R. Gules, E. F. R. Romaneli, and A. Assef, "Transformerless UPS system based on the half-bridge hybrid switched-capacitor operating as AC–DC and DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2173–2183, Mar. 2021.
[28] Y. Hoon, M. M. Radzi, M. Hassan, and N. Mailah, "Control algorithms of shunt active power filter for harmonics mitigation: A review," *Energies*, vol. 10, no. 12, p. 2038, Dec. 2017.
[29] S. Galeshi and H. Iman-Eini, "Dynamic voltage restorer employing multilevel cascaded H-bridge inverter," *IET Power Electron.*, vol. 9, no. 11, pp. 2196–2204, Sep. 2016.
[30] M. A. Mansor, K. Hasan, M. M. Othman, S. Z. B. M. Noor, and I. Musirin, "Construction and performance investigation of three-phase solar PV and battery energy storage system integrated UPQC," *IEEE Access*, vol. 8, pp. 103511–103538, 2020.
[31] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.
[32] M. Inci, "Interline fuel cell (I-FC) system with dual-functional control capability," *Int. J. Hydrogen Energy*, vol. 45, no. 1, pp. 891–903, Jan. 2020.
[33] Y. S. Kanigolla, A. C. Kiran, S. R. Teja, and B. Jyothi, "Reduced switch topologies for multi level inverters with M-carrier SPWM," *J. Crit. Rev.*, vol. 7, no. 2, pp. 623–628, 2020.
[34] C. Subramani, K. Dhineshkumar, and P. Palanivel, "Design and implementation of 13 levels multilevel inverter for photovoltaic system," *J. Phys., Conf. Ser.*, vol. 1000, pp. 20–27, Apr. 2018.
[35] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A square T-type (ST-type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018.
[36] S. T. Meraj, L. K. Haw, and A. Masaoud, "Simplified sinusoidal pulse width modulation of cross-switched multilevel inverter," in *Proc. IEEE 15th Int. Colloq. Signal Process. Appl. (CSPA)*, Mar. 2019, pp. 1–6.

SHEIKH TANZIM MERAJ received the B.Sc. degree in electrical and electronic engineering from the Ahsanullah University of Science and Technology, Dhaka, Bangladesh, in 2015, and the M.Eng. degree from the Department of Electrical and Computer Engineering, Curtin University, Miri, Malaysia, in 2018. He is currently working as a Graduate Research Assistant with the Department of Electrical and Electronic Engineering, University Technology PETRONAS, Perak, Malaysia. He is actively involved in research-based work with specific research focuses on power electronics and applications.

MOHAMMAD KAMRUL HASAN (Senior Member, IEEE) received the B.Sc. degree, in 2003, the M.Sc. degree in communication engineering from the Department of Electrical and Computer Engineering, International Islamic University, Malaysia, in 2012, and the Doctor of Philosophy (Ph.D.) degree in electrical and communication engineering from the Faculty of Engineering, International Islamic University, Malaysia, in 2016. He is currently working as a Senior Lecturer with the Network and Communication Technology research cluster, Center for Cyber Security, Universiti Kebangsaan Malaysia (UKM). He has been experienced working in electrical and communication industries. His undertakings included supervision, installation, and configuration of the corporate information-centric network, servers; WAN, WLAN, LAN, fault handling and programming of the ladder logic design for the industrial LAN connected PLC devices. He has demonstrated excellent research outcomes and received several awards, including Gold medal, scholarships, and best paper. He is well-versed specialist with elements pertaining to cutting-edge information-centric network; wireless communication and networking, microcontroller-based electronic devices, smart grid WAM systems, microprocessor systems, and the IoT. He is a member of the Institution of Engineering and Technology and the Internet Society. He has served the IEEE IIUM student branch as a Chair, from 2014 to 2016. He has actively participated in many events/workshops/training for the IEEE and IEEE humanity programs in Malaysia. He reviews SCIE journals, including IEEE Access, *Telecommunication Systems*, Hindawi, SAGE, *ETRI Journal*, and *KSII Transactions on Internet and Information Systems*.

JAHEDUL ISLAM received the B.Sc. degree in electrical and electronic engineering from the Chittagong University of Engineering and Technology, Bangladesh, and the M.Sc. degree in mathematics (by research) from the Universiti Teknologi PETRONAS, Malaysia. He has experiences with robotics, computational techniques, and machine learning techniques.

YOUSEF A. BAKER EL-EBIARY (Member, IEEE) was born in Cairo, Egypt, in 1980. He received the bachelor's degree in computer science (software engineering) from Modern Academy, Egypt, the High Diploma degree in executive management from The American University in Cairo (AUC), the master's degree in IT from Cairo University, Egypt, the Master of Business Administration from Westbrook University, USA, and the Ph.D. degree in MIS from Cairo University. He is currently working as a Senior Lecturer with the Faculty of Informatics and Computing (FIK), Universiti Sultan Zainal Abidin (UniSZA), Malaysia. He is a member of several committees that related to postgraduate studies, conferences coordination, designing and develop programs. With good experience in administrative work as he held many positions, such as dean of student affairs, faculty's deputy for postgraduate and scientific research, and deputy for scientific research deanship. He was also appointed as an academic advisor and evaluator for postgraduate program, and a consultant in some industries locally and internationally. He has over 11 years' experience as taught various courses both in undergraduate and postgraduate level in many universities around the world conventional and online. He has published more than indexed 150 journal articles, proceedings, and academic books to date in fields information systems, enterprise systems, electronic enterprise, the Internet of Things, theory of computation, and contemporary management. He is also working as the editor-in-chief for research journal and reviewer in several indexed journals. He also leads many international and government research project grants and member in other projects. He has been awarded in many of competition as well as getting intellectual property in some of the projects. He participated more than 50 international conferences worldwide, and due to his vast experience and knowledge, has been invited to a conference chair and delivered his keynote and invited speech at several international conferences. He is a member in many related associations, such as the IEEE, the IEEE Computer Society, IAENG, ACSE, and IACSIT.

JAMEL NEBHEN received the M.Sc. degree in microelectronics from the National School of Engineering of Sfax, Tunisia, in 2007, and the Ph.D. degree in microelectronics from Aix-Marseille University, France, in 2012. From 2012 to 2018, he worked as a Postdoctoral Researcher with LIRMM-Lab Montpellier, France, IM2NP-Lab Marseille, ISEP Paris, LE2I-Lab Dijon, Lab-Sticc Telecom Bretagne Brest, and IEMN-Lab Lille. Since 2019, he has been as an Assistant Professor with Prince Sattam Bin Abdulaziz University, Alkharj, Saudi Arabia. His research interests include design of analog and RF integrated circuits, the IoT, biomedical circuit, and sensors instrumentation.

MD. MOINUL HOSSAIN (Member, IEEE) is currently a Lecturer in electronic engineering with the University of Kent, U.K. He has published over 40 articles including various peer-reviewed journals. He has an H-index of 11 with over 490 citations. His research interests include combustion diagnostics, sensors, instrumentation, measurement, condition monitoring, digital image processing, deep learning, and solid oxide fuel cells. He is an Editorial Member of IEEE Access Journal.

MD. KHORSHED ALAM (Student Member, IEEE) received the B.Sc. degree in computer science and engineering (CSE) in Bangladesh, the master's degree in computer and information engineering (MSCIE) from the Department of Electrical and Computer Engineering (ECE), International Islamic University Malaysia, in 2015, and the Ph.D. degree from the Universiti Teknologi PETRONAS (UTP), Malaysia. He is currently working on a wireless sensor network (WSN) for remote monitoring environmental applications with the Center for Smart Grid Energy Research (CSMER), Institute of Autonomous System, UTP. From 2015 to 2016, he was involved in research under photonic research center with Universiti Malaya (UM). During his master, he worked on wireless resource management for multimedia applications. His research interests include wireless communication (time-series data analysis, time-series prediction, data clustering, data aggregation, and data compression).

NGUYEN VO received the Ph.D. degree from Victoria University, Australia, in 2014. He is currently affiliated as a Higher Education Lecturer and an Internship Coordinator with the Victorian Institute of Technology (VIT), Australia. He is an expert in POS design and development and also in AI research. His research interests include artificial intelligence and power systems.