A Study Of Current Transport Across Metal To Clean Silicon Interfaces

By

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ABSTRACT

A detailed study has been made into the current transport across metal to clean silicon interfaces. The metals considered for the experimental work were gold, chromium, silver and aluminium.

The experimental procedure involved the deposition of the metal film onto the clean silicon surface under ultra-high vacuum (U.H.V.) conditions. Two techniques were used for the attainment of a clean silicon surface. Epitaxial layers were deposited by sublimation under U.H.V. conditions onto heat cleaned substrates and also a straight forward heat cleaning treatment was used in order to produce the required surface. In each case the U.H.V. heat cleaning treatment involved resistively heating the substrate to a temperature of 1200°C for 5 minutes. This technique was essential to the epitaxial layer deposition in order to remove the oxide layer and other contamination and to eliminate any interfacial layer when just considering the heat cleaned surfaces. Cleaving under U.H.V. conditions was considered doubtful due to the residual strain which might distort the surface region.

Due to the fact that intimate metal-silicon contacts are being considered the conventional surface state analysis is definitely not the most applicable in this case. A theoretical model has been developed based on the effects of metal quantum states decaying into the band-gap of the semiconductor. These states are known as quantum tails.

A comprehensive data analysis technique has been used which indicates good agreement between the experimental barrier heights, for both interface formation techniques, and the potential profile in the depletion layer predicted by the model. The variation of barrier height with the various metals used can be explained in terms of the density and distribution of the metal induced surface states in the semiconductor band-gap. Finally the departures of the current-voltage characteristics from the usual approximation of thermionic emission can be explained in terms of the variation of the effective barrier height under differing bias conditions. This effect can be seen to be due to the variations of the charge in the quantum tails under varying bias conditions.

To the author's knowledge this is the first time that data has been reported for metal contacts onto epitaxial silicon layers. Also good correlation has been achieved with the results from the two surface preparation methods.

Further work of interest has been considered with a view to refining the experimental procedure and hopefully producing a more comprehensive understanding of the behaviour at the interface.

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R.A. HEATLEY.

This thesis is gratefully

dedicated to my wife

CLAIRE

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CHAPTER I

INTRODUCTION

1.1. BACKGROUND TO RESEARCH PROJECT

It has long been recognised that the barrier heights of most metal-semiconductor systems do not obey the simple relationship, between metal work function and electron affinity in the semiconductor, put forward by Schottky [1] in 1938. Moreover, it has since been demonstrated, through much experimental evidence, that for many metal-semiconductor systems, including silicon, the barrier heights measured are virtually independent of the metal used. Thus it appeared that there was some other dominant effect, over and above the value of the metal work function, that was causing the Fermi level in the semiconductor to be pinned in the band-gap at the interface.

Tamm[2] was the first to show that the finite size of a crystal lattice must give rise to certain modifications of the band structure. By considering an idealized one-dimensional crystal he found that the boundary conditions of such a system would lead to the existence of allowed levels within the forbidden gap and localised at the surface. A more detailed analysis was put forward by Shockley [3], who was able to show that these surface states could arise from atomic levels and discussed the conditions for their existence.

Bardeen [4] was the first to point out the importance of these surface states in the semiconductor in determining the barrier height. Surface states would cause the barrier height to be largely independent of the metal, for if their density was large enough the contact potential difference would be compensated by the surface charge. However this basic theory and subsequent extensions to it [5] assume that there is an interfacial layer with a thickness of the order of inter-atomic dimensions that can withstand a potential difference.

Heine [6] pointed out that for the case of an intimate metal-semiconductor contact these surface states had no meaning, and that the pinning of the Fermi level at the interface was due to the effects of the metal bulk wavefunctions exponentialy decaying into the semiconductor band-gap.

Inkson [7, 8], on the other hand suggested that the pinning of the Fermi level was due to band-gap narrowing. This pinning is the effect of the screening action of metal overlayers on covalent semiconductors resulting in an upward movement of the valence band edge and a downward movement of the conduction band edge. In addition, Phillips claimed that polarizability effects play the dominant role at metal-semiconductor interfaces. He suggested that it is the elementary excitations [9] and chemical bonding [10] at the interface which determine the behaviour of the Schottky barrier.

Pellegrini [11, 12], Bennett and Duke [13], and Louie and Cohen [14, 15] have all put forward more detailed theoretical analyses based on Heine's initial work, in order to explain the experimental results for barrier heights. There is some doubt about this approach because the barrier height depends to a certain extent on the surface preparation of the semiconductor [16, 17] prior to the metallisation. Whilst silicide forming metals may be expected to give an intimate contact the metallurgical state of the interface is not completely characterised so that a direct comparison of theory with experiment is open to question.

1.2. OUTLINE OF RESEARCH WORK

This project sets out to investigate the current transport across metal to clean silicon interfaces. These interfaces were formed under U.H.V. conditions by the use of two basic techniques. Metal films were evaporated onto epitaxial layers deposited by sublimation, the substrate surface being prepared by a technique of high temperature cleaning. Also considered were metal films directly evaporated onto the heat cleaned silicon substrate surface. Thus it is hoped to obtain atomically clean silicon to metal interfaces in order to obtain information about the evidence of the effect of metallic quantum states tailing into the forbidden gap of the semiconductor. Also a direct comparison can be drawn from the results obtained by the use of the two techniques.

This study has been prompted by the fact that most experimental measurements so far available have been from interfaces in which there is a strong possibility of an interfacial layer, thereby making it difficult to obtain information about the true nature of an initimate metal-semiconductor interface.

Chapter 2 reviews the techniques that have previously been employed in the formation of metal-semiconductor interfaces and also provides a brief historical background to the subject. Chapter 3 outlines the conditions for, and also the meaning of, an atomically clean surface as well as the techniques that can be used in order to determine the surface conditions. This leads to a review of the techniques available for producing a clean semiconductor surface under U.H.V. conditions, This chapter is concluded with a discussion of the most suitable technique for the present work. Chapter 4 describes the majority of the experimental apparatus and techniques associated with the vacuum cleaning of the silicon substrate surfaces and the metallisation procedure. It also includes a description of the vacuum sublimation deposition system which was employed to grow epitaxial films of silicon onto the vacuum cleaned silicon surface. This was employed not only as a technique of producing a metal to clean silicon interface, but also as a technique to determine the success of the vacuum cleaning process, as described in chapter 3.

Chapter 5 describes the actual formation of the metal-silicon devices. The I-V measurement equipment and experimental procedure is detailed in this chapter. All the I-V characteristics obtained for the devices over a wide temperature range are presented in graphical form. Chapter 6 initially outlines the various forms of data interpretation techniquesthat have been employed in metal-semiconductor analysis. The comprehensive data interpretation method used is outlined and the zero bias barrier heights and other information obtained from the I-V results presented.

In the introduction to chapter 7 there is a discussion into the nature of an atomically clean surface as well as the theoretical basis for surface states with energies in the semiconductor band-gap. The conventional surface state analysis is outlined leading to a consideration of intimate metal-semiconductor contacts. The theoretical model developed is presented, based on the effects due to the exponential decay of metallic wave functions into the semiconductor band-gap.

The implications of such a model are discussed with respect to the type of I-V characteristics to be expected.

To conclude with chapter 8 draws a comparison between the experimental results obtained and information calculated from the theoretical model relative to the devices produced. The merits of the theoretical model are discussed in the light of the results obtained from this present work and previously reported data on U.H.V. cleaved surfaces. Then follows a discussion on the results and the various points raised during this work in the light of the previously reported analysis of metal-silicon contacts. Ideas are put forward on further experimental research work that could be carried out as well as extensions to the theoretical model in order to obtain more information about the nature of metal to clean semiconductor interfaces.

CHAPTER 2

A REVIEW OF METAL SEMICONDUCTOR TECHNIQUES

2.1. HISTORICAL BACKGROUND

It is of interest to note that the metal-semiconductor rectifier is the oldest solid-state device, and in fact the first reported experimental work was that carried out by Braun[18] in 1874, who investigated the electrical properties of point metal contacts on lead and ferrous sulphide. The point contact was made by means of a thin wire pressed onto the surface of the crystal and he found that the resistance of the device was dependent on the polarity of the applied voltage as well as the crystal surface conditions. Schuster[19] at the same time made similar experimental observations with contacts onto tarnished copper, which was probably covered with an oxide or sulphide film. There were however, at this time, great difficulties in interpreting this rectification phenomena although Braun did realise that the rectification process was located at the point contact.

The first practical application of these devices was as a detector of high frequency signals in the early days of radio telegraphy[20,21] and many experiments were carried out on devices using lead sulphide[22,23]. However, these devices could not be produced to give constant rectification properties. Also it was found necessary to frequently adjust the point contact in order to maintain useful rectification characteristics. Another problem encountered in these early devices was that hermetic sealing had not been developed so that the characteristics of the devices were affected by the atmospheric conditions.

Gradually the interest in point contact rectifiers turned to silicon and germanium devices. Such devices were used as microwave detectors[24], and were formed by the contact of a tungsten wire onto a polished silicon surface. However, the silicon used in these initial devices was not of the highest purity and consequently their performance and reproducibility was not up to the standard required. Seitz[25] recognised the need for purer silicon for use in these devices, and subsequent devices were made by carefully purifying the silicon and also polishing and etching the surface. Theurer[26] found that the addition of 0.001 per cent of boron to a highly

purified silicon resulted in the production of a highly sensitive crystal. "Boron doping" then became a general practice in these early devices. Most of the point contact devices of this period were formed by a thin sprung wire pressing onto the semiconductor surface with the back contact usually made by means of a solder joint. However, for silicon this was found to be rather difficult and the ground surface was normally metal plated before being soldered.

The importance of etching the silicon surface was recognised for these devices and in fact CP4 etch was first used by Haynes and Shockley [27] in 1951; an etch which is still employed today. It was usually found in these devices that the metal used for the point contact made very little difference to the rectifying properties and tungsten, platinum or platinum alloys were most frequency used. A process which was called "electrical forming" was used in most of these point contact devices and usually consisted of the passage of a large forward current for a short period. This had the effect of reducing the forward resistance and increasing the reverse resistance. This process causes the point contact to penetrate the surface of the semiconductor and leads to a more stable and satisfactory contact.

The effects of the surface conditions of the semiconductor had long been recognised and cleaning as well as vacuum heat cleaning were used as techniques to obtain a better point contact. Also the effects of surface defects, induced by mechanical polishing, were noted. Other techniques used for the preparation of semiconductor surfaces were neutron bombardment [28] and positive ion bombardment[29]. These techniques were found to produce surfaces which formed better point contact devices, although the exact effect that they had on the semiconductor surface was not understood.

Rolka, Jackson and Ulrich [30] were the first to describe a metal semiconductor contact formed by vacuum evaporation of the metal. In their devices the germanium slices were covered with a varnish and the metal evaporated onto the surface through holes pierced in the varnish. These devices showed better rectification properties and were far more mechanically stable than the point contact devices. Thus this development and the recognition of the need to clean the semiconductor surface were the first steps towards the modern approach of the formation of metal-semiconductor contacts.

2.2. MODERN RESEARCH TECHNIQUES

There has been considerable interest shown in the study of metal semiconductor interfaces in recent years in the form of both experimental and theoretical research. This can, to a certain extent, be attributed to the development of recent ultra high vacuum techniques which now make it possible to form a clean silicon surface under U.H.V. conditions immediately prior to the evaporation of a metal film. Thus it has become feasible to produce an ideal metal to semiconductor interface, and these techniques are fully described and discussed in chapter 3.

This means that the ever growing new theoretical analysis of the behaviour at the interface of an intimate metal semiconductor contact[6-15] can now be experimentally investigated. However prior to the development of these U.H.V. techniques, the normal practice was to employ some form of chemical cleaning process to the substrate surface in order to remove the surface oxide layer and any other surface contamination that might be present. The metal would then be deposited onto this chemically cleaned surface at a pressure of typically 10^{-7} torr.

Turner and Rhoderick[16] carried out an investigation into the characteristics of metal-silicon contacts, where the silicon surface had been prepared by several different cleaning processes. The chemical etches used were a mixture of hydrofluoric and nitric acid in ratios of 1:8 as well as 1:3, also CP4 was used. Other techniques used were based on oxidation followed by an hydrofluoric acid etch. The oxidation was achieved either by thermal oxidation or anodic oxidation in a solution of boric acid and sodium tetraborate. In all the above cases the procedure was followed by ultrasonic washing in deionised water, acetone and methonol, and the slices stored under methanol, to prevent any oxide growth, until required. These various cleaning procedures are typical of those employed in the surface preparation of substrates for subsequent formation of Schottky barrier devices, and in all cases devices with good rectification properties will be produced.

With regards to the actual formation of the devices; the metal film was evaporated through a mask to produce the dots in a working pressure of 5×10^{-8} to 10^{-6} torr. This technique of using a mask is perhaps the most common for the production of metal contacts. The mask has to be in very close proximity to the substrate surface, during the evaporation in order for well defined dots to be produced. This proximity can give rise to undesirable contamination effects.

An alternative technique which can be used is to photoengrave and etch the metal film in order to produce the dot pattern. This technique is probably more desirable as in this case the metal-semiconductor contact has already been formed, thus reducing the possibility of any interfacial contamination.

For device measurements it is obviously essential to ensure that a good ohmic back contact is formed to the substrate, and this can pose severe problems in order to produce a chemically stable contact with virtually no inherent impedance to current flow. A detailed analysis of this problem has been made by Lepselter and Andrews [31] by the investigation of transition metal silicide contacts. This technique of the formation of a metal silicide contact produces the best ohmic characteristics and is usually achieved by the evaporation of the metal onto the silicon surface and subsequent sintering in order to form the alloy. Various transition metals or B-subgroup elements can be used for this purpose. Perhaps the most common used in metal-semiconductor research is gold antimony.

When an intimate metal-semiconductor contact is to be considered, chemical cleaning alone will not be sufficient. An interfacial oxide layer of at least 5A° thickness will be present if no subsequent vacuum cleaning technique is employed. This has to be the case in the majority of experimental work so far undertaken.

Cleaning of silicon blocks under U.H.V. conditions, in order to produce a contamination free surface, is the only technique which has been given any real consideration. The process usually undertaken consists of chemical cleaning of the silicon blocks and the formation of an ohmic contact before being placed in the U.H.V. system. The block, which is scribed along the cleavage plane is mounted in a holder so that a knife edge can be struck against the scribed line in order to produce a clean surface under U.H.V. conditions. The metal can then be evaporated through a mask in order to form the dots on the freshly cleaned surface. By using this technique it is possible to form a metal to clean silicon interface at pressures below 10^{-10} torr.

Turner and Rhoderick[16] also used this technique but not at such low pressures, and the characteristics of the devices produced showed poor rectification properties. Spitzer and Mead[32] used vacuum cleaning in an investigation into the characteristics of metal to CdS and Ga As interfaces. In their case evaporation of

the metal, at a pressure of 5×10^{-7} torr, was commenced before the crystal had been cleaned in order to eliminate the possibility of contamination of the crystal surface by the residual gases present in the vacuum system.

U.H.V. techniques have advanced still further in recent years with the capability of actually carrying out electrical measurements on the devices formed without breaking the ultra high vacuum. Van Otterloo and De Groot [33] have measured the current-voltage and capacitance-voltage characteristics of Ag-silicon diodes formed by cleaving and evaporation of the metal film through a mask, under U.H.V. conditions. The temperature at which the measurements were made could also be varied by the passage of different liquids through the substrate sample holder.

Problems arise in the interpretation of barrier height data because of the uncertainty of the correct values of the various metal work functions. These are generally taken from published data and usually refer to experimental conditions quite different from those under which the metal film has been evaporated. Relating to this, it should be noted that only the highest purity metals should be used and these should be given a chemical cleaning treatment, in order to remove surface contamination, before being placed in the U.H.V. system.

Thanailakis[34] has undertaken an investigation into the characteristics of various metal to silicon interfaces formed by cleavage at a base pressure of 5×10^{-11} torr. He used an in situ technique for comparing the work function of the cleaned silicon surface with a stainless steel reference electrode. This comparison was made by means of the Kelvin method of measurement of the contact potential difference between the vibrating steel reference electrode and the cleaned silicon surface. The metal film was then evaporated through a mask to produce the dot array and the metal work function determined in a similar fashion. After these measurements the barrier heights were determined by measuring the current - voltage, capacitance-voltage and photoelectric characteristics of the contacts. This is a very valuable technique as all the measurements necessary can be determined under the same experimental conditions as used in the contact formation.

Thus it can be concluded that the experimental techniques related to the investigation into the nature of metal-semiconductor interfaces have advanced considerably. It would now appear that measurements can be made on near ideal intimate metal-silicon contacts although reservations should be placed on the cleaving technique as this cannot be considered to produce reliably the ideal silicon surface structure[33] as will be discussed in the following chapter.

CHAPTER 3

CLEANING OF SILICON SURFACES AT U.H.V.

3.1. INTRODUCTION

As this work is primarily concerned with obtaining a greater understanding of the nature of metal contacts onto atomically clean silicon surfaces, it is very important to establish a technique that will reliably and also consistently produce a clean silicon surface at U.H.V. prior to the deposition of the metal film. The technique must also maintain good lattice conditions up to the surface, that is, free from steps or strain.

In this chapter we will outline the basic concept of what is meant by an atomically clean surface, and the techniques that can be employed in order to produce such a surface. The reasons for adopting the particular techniques used in this present work will then be discussed.

3.2. CONDITIONS FOR A CLEAN SILICON SURFACE

All freshly cut silicon substrates require a series of mechanical lapping and polishing operations, followed by a final chemical polishing and/or gas polishing to remove oxides as well as the thin mechanically worked region[35]. While this polishing helps to maintain a uniform finish and produces a shining, polished appearance, the resulting substrate surface cannot be produced completely free of imperfection and contamination[36].

By an atomically clean surface we mean one free of all but a few per cent of a single monolayer of foreign atoms, either adsorbed or substitutionally replacing surface atoms of the parent semiconductor lattice. It has long been recognised that the cleaning of a solid surface is a three-dimensional problem since contamination effects may extend over several atomic layers. It is therefore of importance to consider what are the factors that contribute towards causing the semiconductor surface region to deviate from the ideal form. This in itself poses various problems as Lander and co-workers have shown that the silicon (111) surface may exist in a number of different forms depending on the methods of cleaning[37,38] used. Models for the surface structure of clean silicon will be discussed more fully in chapter 7.

In this chapter the causes of surface contamination will be discussed together with the techniques that are available for the determination of surface cleanliness.

The deviations from an ideal semiconductor surface can be attributed to a number of causes including substrate surface damage[36] and contamination[39] as well as thermal[40] and mechanical stress. Furthermore the surface could become contaminated during the deposition of the metal film. The two main contaminants to be considered as far as a silicon surface is concerned are oxygen and carbon[41,42] Analysis of bulk material shows that both of these elements are contained in silicon in varying amounts[43,44] but higher concentrations than can be accounted for by segregation arefrequently observed at the surface[45,46]. A clean silicon surface exposed to air will rapidly form an oxide film 10-30A° thick which increases slowly in thickness with time[47]. Carbon contamination may arise from polishing contamination or adsorption of carbon containing impurities from the air or from reagents used for the surface preparations[45]. Thus one must make sure that the silicon surface is as free as possible from these contaminants.

A number of techniques are available for determining the surface character and cleanliness. These include Auger electron spectroscopy,[48] low energy electron diffraction (L.E.E.D),[49,50] high energy electron diffraction (HEED)[51], surface replica electron microscopy[52] and ellipsometry[53]. However apart from electron microscopy, these techniques were not readil y available during this work. As epitaxial layers of silicon could be grown by sublimation under U.H.V. conditions onto the clean silicon surfaces, this provides a very useful technique for establishing whether or not the cleaning process used does in fact produce an atomically clean surface. This is due to the fact that it is well established that the quality of the epitaxial layer grown in this manner is very dependent on the surface cleanliness of the silicon substrate[36]. An oxide film on the silicon substrate surface will inhibit the growth of a silicon epitaxial layer. This is observed by the existence of an induction period, which is the time taken for the removal of the oxide film by reaction with silicon from the vapour stream[53], or, at high temperatures, from the substrate[36]. However, at low arrival rates of silicon the presence of an oxide on the substrate surface will impede single crystal growth, while high arrival rates swamp the oxide[55], trapping it, causing defects to form in layers originating at the trapped oxide centres. Carbon contamination is however a more serious problem since carbon readily reacts with silicon at elevated temperatures to produce silicon carbide. Silicon will not

nucleate upon silicon carbide[56] and so, if present, nucleation will only occur on clean silicon regions in the surrounding silicon carbide. This leads to three dimensional nucleation[55,57], and the silicon carbide is swept across the surface by the growing centres to form defects in the grown lattice which may result in the existence of stacking faults, twinning, and faceting. However, no three dimensional nucleation is observed on a clean silicon surface. Thus a study of the crystalline perfection of the resultant grown layers can provide a very good test as to the success of the technique used for the cleaning of the silicon substrate surface. The details of the silicon sublimation experiments and methods used to establish the crystalline perfection of the epitaxial layers is discussed in chapter 4.

3.3. TECHNIQUES AVAILABLE FOR PRODUCING A CLEAN SILICON SURFACE UNDER U.H.V. CONDITIONS

There are three basic well known techniques that can be used to produce a clean semiconductor surface under U.H.V. conditions and these are:

(a) Positive ion-bombardment with ions of an inert gas;

(b) Cleaving of the semiconductor surface;

(c) High temperature heat cleaning.

In this section we will review the processes involved in all of these techniques as well as discussing their relative merits with regards to the present work.

3.3.1. POSITIVE ION-BOMBARDMENT

One convenient way of both cleaning the surface of a crystal and also removing material in a controlled fashion is by positive ion-bombardment. This process basically involves the bombardment of the surface with medium to low energy (0.2keV - 2.0) inert gas ions followed by annealing at approx 700°C. The bombardment ions, which remove the surface contamination, are usually formed by the acceleration of electrons from a filament in a pressure of argon 10^{-4} torr. The subsequent annealing serves to restore the surface crystalline structure.

Dillon and Farnsworth have carried out a series of experiments using LEED techniques on germanium crystals cleaned by the use of ion bombardment[58]. In their experiments the germanium substrates surfaces were chemically etched before being placed in a U.H.V. system capable of a base pressure of 5×10^{-10} torr.

The experimental procedure used for obtaining a clean surface was to repeat cycles of about 20 hours of heating at 650°C for outgassing followed by ten minutes of ion bombardment and fifteen minutes of annealing at 500°C until there was a cumulative ion-bombardment time of 90 minutes. An ion-bombardment current of 60 - 100μA at a voltage of 400 - 500V was used in a pressure of argon of between 5×10^{-4} and 3×10^{-3} torr. The LEED results obtained for the surfaces produced using this procedure showed no evidence of ion-bombardment induced etching defects. Microscopic examination of the surface showed no evidence of preferential etching of the type reported by Wehner[59] for metal single crystals.

Farnsworth and co-workers also carried out similar experiments on (110) silicon crystal surfaces[60]. As before the substrates were given a chemical etch before being placed in the U.H.V. system. It was found that in order to produce a LEED pattern consistent with a clean silicon surface it was necessary to heat the crystal at 900 - 1100°C for about 250 hours and ion-bombard the surface for a total of seven five minute periods at 100μA ion current at a potential of 400V. Following each ion-bombardment at room temperature the crystal surface was annealed at 700°C or higher for 5 to 15 minutes. Law[61] used positive ion-bombardment in order to vacuum clean silicon substrate surfaces and measured the following characteristics in order to determine the state of the surface during various bombardment and annealing processes.

(a) Conductivity

(b) Photo-conductivity

(c) ΔCP, the change in contact potential of the surface with light

The conclusion from this experimental work was that a surface which was clean in a three-dimensional sense could be produced with sufficiently heavy ion-bombardment, and that the time required in order to anneal out the surface damage varied from 15 minutes at 1580°K to about 700 minutes at 1020°K.

Thus from the experimental evidence it would appear that by a careful control of the outgassing procedure, the ion-bombardment energy and duration as well as the anneal temperature, a contamination free semiconductor surface can be produced. It is however doubtful as to whether the crystallographic damage due to the ion-bombardment can be completely annealed out.

3.3.2. VACUUM CLEAVED SURFACES

Vacuum cleaving of crystals provides a very good technique of obtaining instantaneously a contamination free surface at any desired temperature. However, the most important factor, when cleaving is to be considered, is the flatness of the resultant layer produced and also the effects of the mechanical stress on the surface lattice structure.

Henzler[62] carried out a series of experiments on vacuum cleaved silicon surfaces using LEED to detect regular and irregular step arrays and to derive step height, terrace width and step orientation. LEED is very useful in this case as it has been shown to be sensitive to many deviations from an ideal surface[63]. Also employed was the use of optical reflection to study and determine the inclinations of a light beam reflected at the surface of the cleaved crystal. Due to the inclined portions of the cleaved surface a small diameter light source is expanded into a pattern which is characteristic of the deviations from the ideally flat surface and is called the inclination pattern. From the LEED results the cleaved silicon (111) faces showed regular and irregular step arrays with step edge in the (110) direction.

The observed height has always been close to that of the minimum for one double layer (3.14A^{o}) as suggested by crystal structure. From the optical reflection patterns, the angle of inclination of the silicon cleaved faces toward (111) vary generally from 0 to 5^{o}. He also found that the spatial distribution of the inclined zones was not uniform. From scanning the surface with LEED to investigate the superstructure of the freshly cleaved surfaces, he found the silicon (2 x 1) superstructure usually associated with cleaved surfaces. The superstructure changes irreversibly, by heat treatment of 370^{o}C and above, to the (7 x 7) superstructure. This would tend to suggest that the (2 x 1) superstructure is unstable and that the (7 x 7) superstructure is an intrinsic silicon structure. Also Henzler noted the disappearance of atomic steps as the (7 x 7) superstructure developed. This again brings us onto the question of the surface structure of clean silicon which will be more fully discussed in chapter 7.

Aspnes and Handler[64] have also carried out investigations into cleavage induced defects and they concluded that silicon does not have a great tendency to cleave in the (111) plane and consequently there will be inevitable non-uniformities present on any large cleaved surface. These can be mainly divided into two

categories, the macroscopic imperfections such as steps or cracks and the microscopic defects such as local lattice disorder. Thus it would appear that it is extremely difficult to produce a cleaved surface that is free from the surface imperfections mentioned, certainly on a large scale.

It is clear that cleavage gives rise to a surface that is not crystallographically ideal. This fact makes the interpretation of data obtained from this method, of doubtful value so that the work of Thanailakis[34] may need re-appraisal.

3.3.3. HIGH TEMPERATURE HEATING

The technique of high temperature cleaning basically involves the heating of the silicon substrate, to near its melting point in order to remove the unwanted impurities. Chang[45], using a LEED - Auger system, has investigated the effects of heat treatment on silicon substrates. He mentions that if the surface is heated to progressively higher temperatures, the gradual disappearance of first oxygen at 900 - 1000°C and then carbon at 1100 - 1200°C can be followed. If there are any heavy metals present such as Fe, Cu and Ni then these will rapidly diffuse into the bulk at these temperatures[65]. Thus the indications are that most unwanted impurities can be removed by simply heating to 1200°C under U.H.V. conditions. These results have been correlated with the nucleation of silicon epitaxial films, in that, the presence of oxygen is associated with an induction period [66] during which no film is deposited, and the presence of carbon causes the growth of three di mensional nuclei[67]. Also other Auger studies[68-70] have shown that a silicon substrate cleaned by heating to 1200°C at U.H.V. can be free from impurities to within the detection sensitivity of the Auger technique (1 to 3% of a monolayer coverage). Silicon substrate heat treatments of above 1200°C have been shown to produce the appearance of metallic impurities at the surface[45], which obviously would not be desirable.

Gale[36] carried out an investigation into the optimum temperature and time for vacuum heat cleaning silicon substrates with a view to producing a surface which allows subsequent low defect density silicon epitaxial layers to be grown. He observed the nucleation process of the silicon epitaxial layers after substrates had been subjected to a heat treatment ranging in time from 5 minutes to 30 minutes and at temperatures of between 1100°C and 1200°C. By this technique and also the use of LEED he determined that the optimum time and temperature to ensure the removal of the oxygen and carbon contamination

from the surface and also to produce a LEED silicon (7 x 7) pattern was 5 minutes at 1200°C. However in order to achieve such a short period of heating it was found necessary to etch the substrates in hydrofluoric acid for one hour prior to being placed in the U.H.V. system. Parish[71] used the same heat treatment technique for experimental work on the growth of silicon epitaxial layers by sublimation at U.H.V. and was able to produce very low defect density epitaxial layers. Thomas and Francombe[72] also used heat cleaning at 1200°C with resultant sharp LEED patterns characteristic of a clean silicon surface. They were able to grow very good quality epitaxial films by sublimation onto substrates prepared in this manner.

Many other workers[54,73] have also used this technique successfully in order to produce clean silicon surfaces under U.H.V. conditions. Thus heat cleaning of silicon substrates provides a very quick and easy technique of obtaining a clean surface at U.H.V. It has been used by many experimentalists to produce a surface for subsequent epitaxial of silicon layers [74-76] and as mentioned earlier in this chapter it is essential for the substrate surface to be free of contamination in order for this process to be successful. The work of Parish[71] on the segregation of impurities indicates that there should not be a significant variation of impurity density due to the thermal cleaning technique.

3.4. DISCUSSION

As this work entails an investigation into the current flow across metal to clean silicon interfaces it is essential to be able to prepare clean surfaces of silicon. The results of such a study can then be useful in understanding the behaviour of contacts prepared under more usual conditions. It is well known that surface lattice defects and irregularities will contribute towards the surface state density, thereby affecting the barrier height which determines current flow in the contact. This has been well illustrated by Van Otterloo and DeGroot[33] in their investigation into silver contacts on cleaved silicon surfaces. From the experimental results they found that the barrier heights of the contacts formed were very dependent on the quality of the cleaved surface. Also it has been shown that macroscopic distortion on cleaved silicon surfaces can form preferential current flow lines[64]. Thus it would appear that perhaps cleaving is not the most ideal technique to be used when considering metal to clean silicon interfaces

due to the uncertainty of the effects of surface irregularities on the barrier heights and the current flow in the devices.

Ion-bombardment usually necessitates a rather lengthy process and the optimum time and energy to be used in order to produce a clean surface has been reported differently by various research workers. This tends to make the technique perhaps rather uncertain and dependent on the experimental arrangement. Also the ion-bombardment induced surface defects, which are not completely annealed out, would produce similar effects as those mentioned for the cleaved surfaces. As far as the author knows ion-bombardment cleaning of silicon surfaces at U.H.V. has not been used for any metal-silicon interface analysis.

It has however been well demonstrated that heat cleaning of silicon surfaces at U.H.V. will provide a contamination free surface with a minimal of surface defects. Recently however Mottram, Thanailakis and Northrop[77] have reported the formation of a p-type layer on the surface of n-type silicon substrates heated to 1200°C. This was discovered during work on metal to clean silicon interfaces when it was noted that heat cleaning of the silicon surface before the metallisation resulted in devices with very poor rectification characteristics. It was further found that the p-type layer was of the order of microns thick and in some cases could be more heavily doped than the substrate. This effect does seem rather unlikely and no real explanation could be put forward. In the present work a series of experiments were carried out, whereby vacuum heat cleaned silicon slices were thermally probed in order to determine the conductivity type of the surface. In no case was there found to be any evidence of the formation of a p-type surface layer. Also this phenomena has not been observed in any of the research work on epitaxial layers grown by sublimation onto vacuum heat cleaned surfaces. An ion pump has been used in the present work as opposed to a diffusion pump. This might tend to suggest that the group III impurities were being released from the xeolite trap during the bake out and heat cleaning procedures.

As heating at 1200°C for five minutes will produce a surface that will allow subsequent good quality epitaxial layers to be grown, we consider this technique suitable in order to produce the clean silicon surfaces required in this experimental work. Also as it has been well demonstrated that good quality epitaxial layers can be grown onto heated cleaned surfaces[36,71] this would seem to be an ideal

technique for providing a clean silicon surface prior to the metallisation. The importance being the fact that a freshly grown surface under U.H.V. conditions would be available thus eliminating the doubts of contamination from surfaces which have to be cleaned in some manner.

CHAPTER 4

EXPERIMENTAL TECHNIQUES

4.1. VACUUM EQUIPMENT

The metal to clean silicon interfaces were formed in a Vacuum Generators 140B, general purpose stainless steel vacuum system. Pumping of the system was achieved by an Edwards ED100 two stage rotary pump, with a sorption foreline trap, for roughing to a pressure of about 10^{-3} torr. The foreline trap was necessary in order to provide oil free conditions in the vacuum system, as any residual pump oil present in the system could lead to carbon contamination of the silicon surfaces[36]. A molecular sieve sorption pump was then employed as an intermediate pump to achieve a pressure of about 10^{-4} torr; this pressure was low enough to start a 140 litre/second Ferranti getter-ion pump, model FJD 140, which was used to produce the ultra high vacuum conditions. The ion pump was connected directly to the system at the base of the service well giving an effective pumping speed close to the speed of the pump[78]. The only possible disadvantage with the pump in this position was that it became exposed to atmospheric pressure when the system was opened; however, this exposure appeared not to affect the ion pump performance throughout the whole project. A bakeable valve could be used to isolate the ion-pump when the system was at atmospheric pressure, however as the valve conductance is typically 100 litres/second the effective pumping speed would be reduced by more than a half[79]. If a bakeable valve was employed the ion-pump could be assisted by a titanium sublimation pump, but this form of pumping can lead to the release of uncontrolled amounts of contamination. In theory, however, base pressures of $< 10^{-10}$ torr are obtainable if the pumping speed is $>$100 litres/second[79], so the uncertainties of a sublimation pump were avoided by situating the ion pump at the base of the service well. A stainless steel table was mounted in the system in order to prevent titanium from the ion pump being sputtered into the experimental working region, and also to prevent any material from falling into the ion pump. This table caused a negligible reduction in the pumping speed. Pressures were measured by

a Vacuum Generators VIG20 Bayard-Alpert ionisation gauge. Base pressures of $<2 \times 10^{-10}$ torr were possible after baking at 250°C to thoroughly out-gas the chamber walls and system components. The optimum bakeout period was found to be six hours and figure 4.1. shows the pressure during a typical pump down/bakeout sequence. The sequence was controlled such that the pressure was not allowed to rise above 10^{-5} torr, so as to keep to a minimum any contamination of the silicon surface during the bakeout period. A G.W.B. quadrupolemass spectrometer was installed in the vacuum chamber in order to monitor the residual gases present during the various experimental procedures. Typical mass spectra are shown in figure 4.2. for the various cases listed below.

(a) After the system has been pumped down and baked out to a pressure of 5×10^{-10} torr.

(b) During the high temperature heat cleaning of the silicon substrate at a pressure of 5×10^{-9} torr.

(c) During the metallisation of aluminium at a pressure of 5×10^{-9} torr.

4.2. SILICON SUBSTRATE DETAILS

The silicon substrates used in this project were cut from 32mm diameter Czochralski grown slices of 0.2mm thickness, with one side commercially polished; in all cases the slices were manufactured and polished by either Texas Instruments or Monsanto. The slices had been prepared for normal epitaxial deposition by a chemical vapour technique[35] with an orientation 1-2° off the (111) axis because this offers advantages for silicon epitaxial growth [35,55]. The dislocation density in all slices was ≤ 2000 cm^{-2}. The substrate doping type and concentration was chosen according to the experiment being undertaken; the lowest resistivity slices available, the order of doping density 8×10^{18} cm^{-3} Antimony, were used when an epitaxial layer was to be grown, and higher resistivity slices $\sim$10ohm cm were used when the metal film was to be deposited onto the heat cleaned surface. The 10 ohm cm resistivity slices had previously been given a back N^+ diffusion in order to produce the basis for a good ohmic back contact when considering the characterisation of the devices. In all cases the resistivity of the slices was measured by the four-point probe technqiue [80].

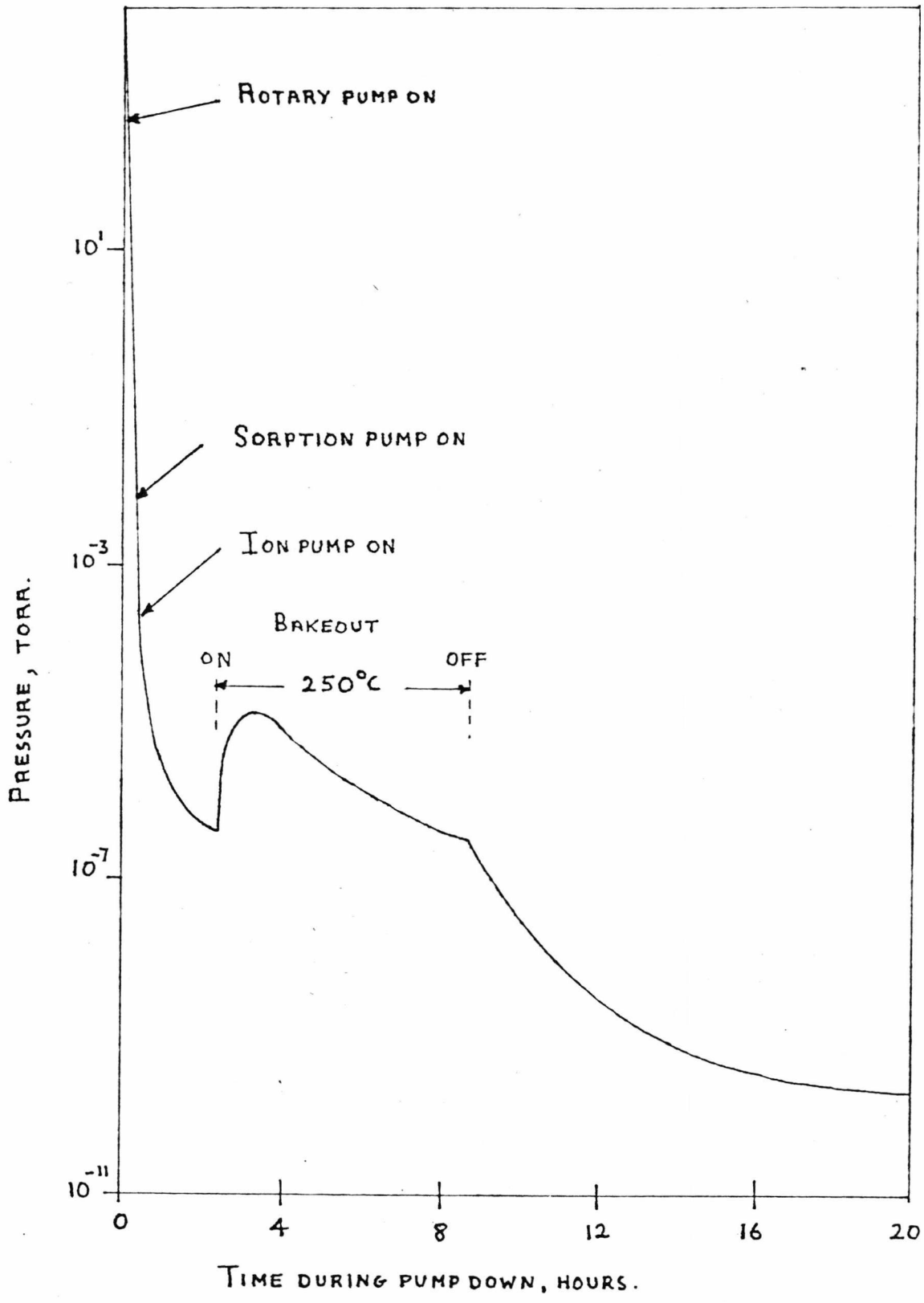


FIGURE 4.1 : VACUUM PRESSURE AS A FUNCTION OF TIME DURING PUMP DOWN.

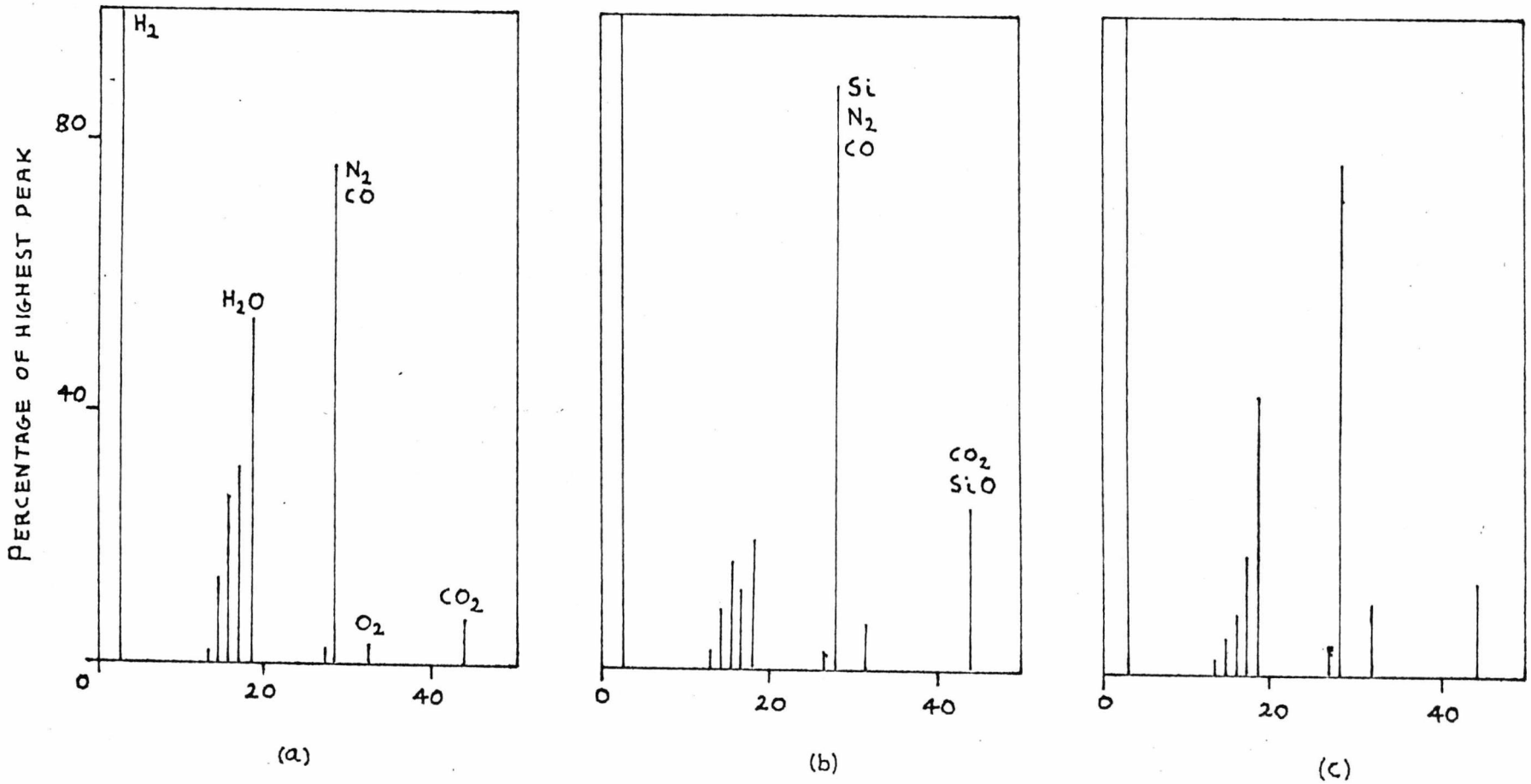


FIGURE 4.2 : MASS SPECTRUM OF THE VACUUM CHAMBER RESIDUAL GAS FOR VARIOUS CONDITIONS.

The substrates were cut from the silicon slices by scribing with a diamond stylus, and then cracking the slice along the scribed lines by rolling a rod over the back of the slice with the polished face resting on a stack of filter papers. The dimensions of the substrates used were 19 x 7.5mm as this was found to be the largest size of substrate that could be uniformly heated in the substrate holder/heater used. Substrate heating at U.H.V. was not only necessary in order to clean the silicon surface, but also to maintain the substrate at a constant temperature during the epitaxial growth. This was achieved by the passage of an A.C. current directly through the substrate (resistive heating) with the substrate mounted in the holder/heater shown in figure 4.3. The substrate was mounted between two tantalum clips, with support being provided by a re-crystallised alumina platform running parallel to and behind the substrate. Four silicon blocks were used to separate the substrate from the alumina platform and from the tantalum clips. These were used in order to prevent contamination from the alumina, and also to reduce the risk of tantalum contamination reaching the substrate[78], as the increase in silicon cross-sectional area at the block positions lead to a reduction of the heating effect at the tantalum clips. The silicon blocks were always cut from the same slice as the substrate thus preventing any other unwanted impurities from reaching the substrate surface.

The whole substrate holder/heater assembly was mounted on a Vacuum Generator U.M.D.1 universal rotary drive situated at the top of the vacuum chamber. The electrical contact was made by thick copper leads connected between the tantalum clips and the electrical feedthroughs in the rotary drive assembly. This allowed 300° rotation of the holder/heater and enabled the substrate to undergo the necessary high temperature heat cleaning procedure screened from the silicon source and the metal evaporation source. The substrate could then be subsequently positioned above either source when required. The same heat cleaning procedure was used to prepare the surface for subsequent epitaxial growth and for the metal to heat cleaned silicon interface formation.

4.3. SILICON SOURCE DETAILS

The source material, manufactured by Hoboken, was Czochroski grown silicon of (111) orientation in 1mm thick slices. The source material was uniformly doped with phosphorus where the impurity concentration was measured by the four point

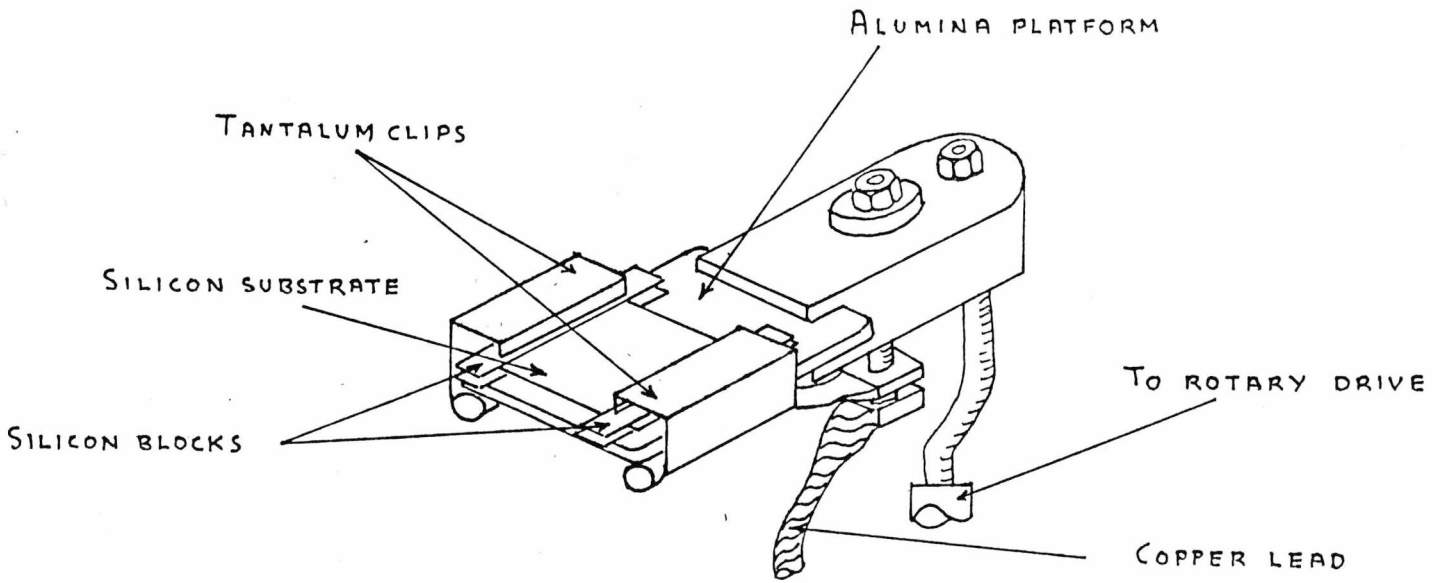


FIGURE 4.3 : SILICON SUBSTRATE HOLDER/HEATER.

probe technique[80]. The four point probe technique is described in Appendix A and the impurity concentrations could be evaluated to an accuracy of about ±2%. The slices were cut, using a diamond wheel, into bars of dimensions 4mm x 15mm x 1mm. and four 4mm x 4mm. blocks were also cut from the same slice. The silicon bars and blocks were given an ultrasonic wash in methanol to remove any grease and soluable deposits. The silicon bars were then mounted back to back, via the four silicon blocks, between two tantalum clips . This structure was given support by alumina sections running between the tantalum clips either side of the silicon source. This structure produces a narrow source region of cross section 4mm x 2mm for a 10mm length, between block positions, as shown in figure 4.4. So, when the source was resistivly heated, the narrow region became considerably hotter than the rest of the structure, thus allowing high sublimation rates only from the narrow region. In this way the possibility of contamination from the tantalum contacting clips was minimised; also the vapour pressure of tantalum at the source (and substrate) temperatures used in these experiments is extremely low[78].

The source was arranged so that one wide face (4mm width) of the sources narrow section was directly underneath and parallel to the substrate (in its deposition location), with a source-substrate distance of 15mm. The source assembly was mounted in the vacuum chamber via thick copper connections between the tantalum clips and electrical feed throughs on the vacuum system.

In order to heat the silicon by the passage of current it was necessary (1) to use a low current, high voltage supply to warm the silicon thus reducing its resistivity[81] then (11) to switch to a low voltage, high current supply to produce sufficient current to heat the silicon once the resistivity has fallen. The basic diagrams of the current supplies used for the source and substrate heating are shown in figures 4.5(a) and 4.5.(b).

4.4. THE METAL EVAPORATION SOURCE

The metal evaporation source used during this work consisted of a small tantalum basket with a graphite insert. The dimensions of the graphite crucible was 4mm diameter x 4mm in depth. This crucible was machined from a block of graphite and given an ultrasonic wash in methanol before being placed in the U.H.V. system. The metal evaporation source was positioned parallel to the silicon source at a distance of 10cms below the silicon substrate holder. The tantalum basket was mounted via thick copper connections to electrical feedthroughs in the vacuum system.

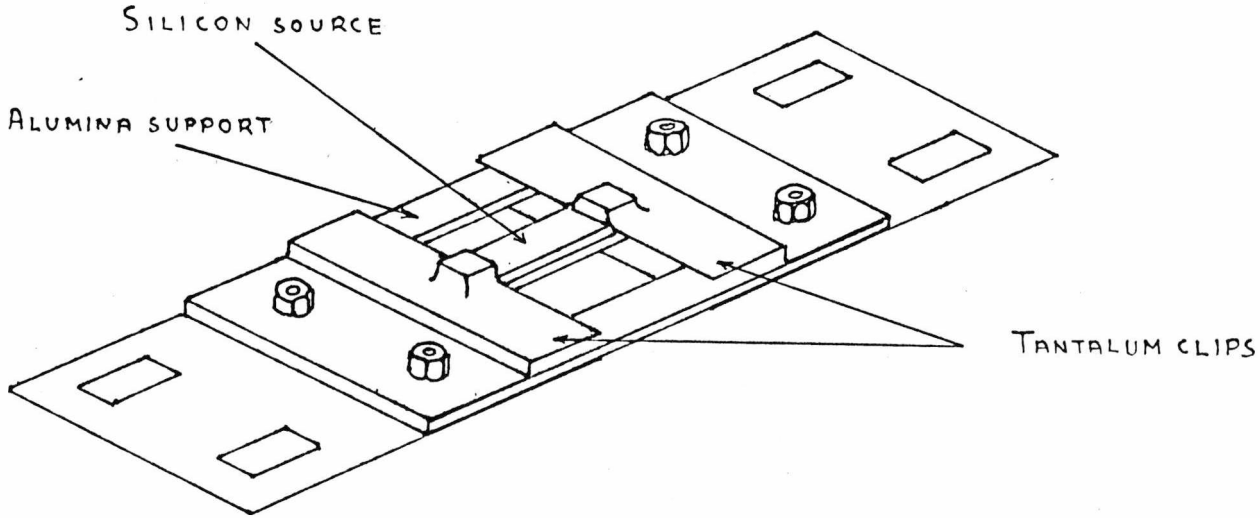
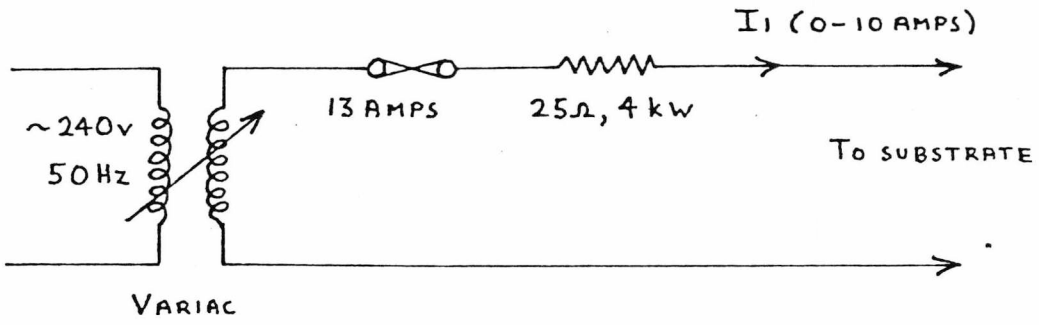


FIGURE 4.4 : SILICON SOURCE HOLDER/HEATER

POWER SUPPLY FOR SUBSTRATE HEATING



POWER SUPPLY FOR SOURCE HEATING

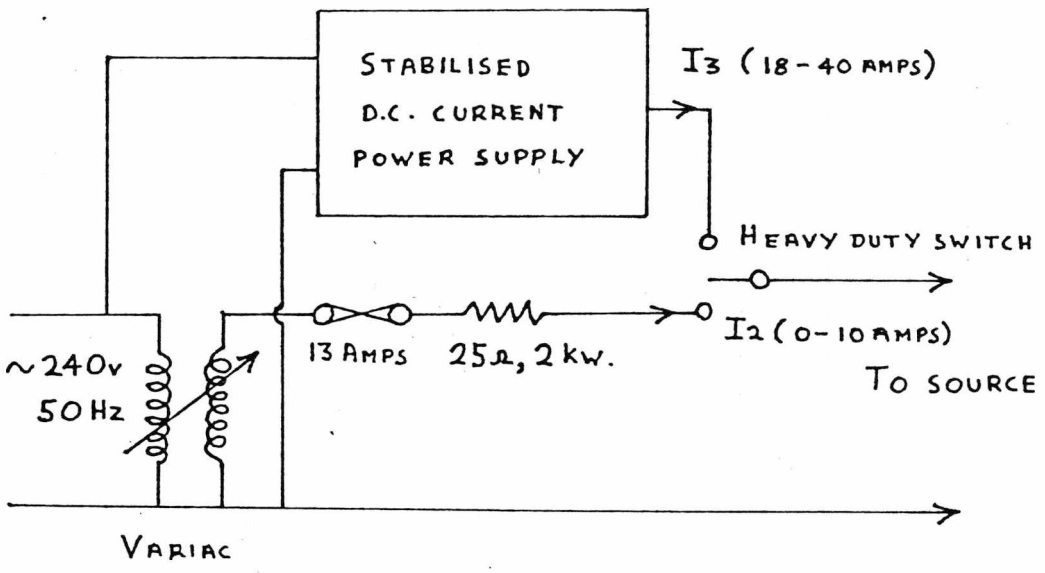


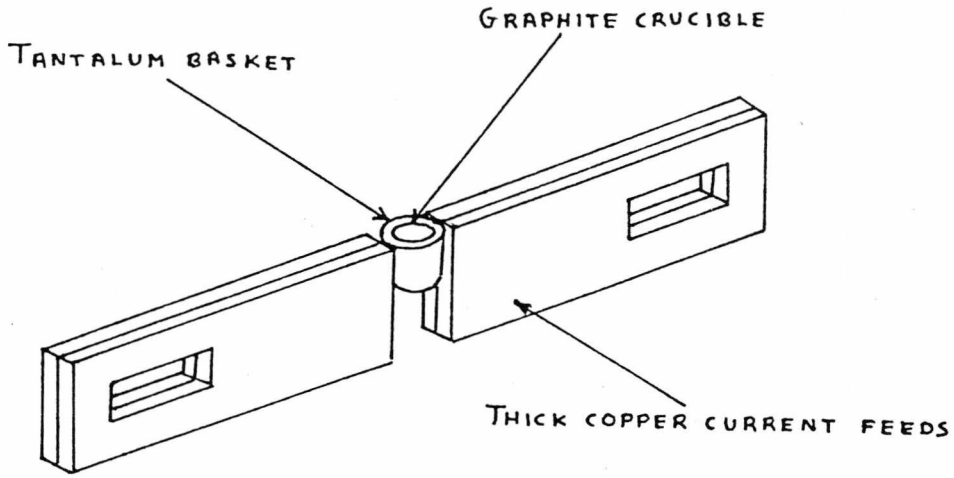
FIGURE 4.5 : DUAL CURRENT POWER SUPPLIES FOR HEATING SUBSTRATES AND SOURCES

The graphite crucible was found necessary as, during preliminary experiments, it was discovered that the metals being used seem to form some kind of alloy with the tantalum, when heated, causing the tantalum basket to become brittle and finally fracture. Also the use of the graphite crucible lead to a more uniform heating of the metal. This evaporation source provided a good U.H.V. performance with all the metals used, causing a minimal pressure rise during operation. A Vacuum Generator E.G.2 U.H.V. electron beam evaporation source was also used but this was found to lead to an undesirable pressure rise. The metal evaporation source and power supply arrangements is illustrated in figure 4.6.

4.5. U.H.V. SUBLIMATION TECHNIQUES

The silicon sublimation techniques used in this project were those as employed by Parish[71] in his investigation into the incorporation of impurities into epitaxial layers grown by sublimation under U.H.V. conditions. Using the silicon substrate and source arrangement as described, it is possible to grow epitaxial layers at substrate deposition temperatures of between 500°C and 750°C. It has been shown [36] that using substrate temperatures $<$750°C results in negligible out diffusion of impurities from the substrate into the grown layer. The sublimation rate is controlled by varying the current through the silicon source, in this way temperatures of between 1300°C and 1400°C were achieved at the narrow region. This deposition arrangement will result in a uniform sublimation rate over the whole silicon surface[82], and substrate epitaxial growth rates of between 0.2 and 1.6 μm/hr were obtainable by varying the source temperature and this is illustrated in figure 4.7.

Temperatures of the substrate of below 800°C were measured by a Pt-Pt/Rh thermocouple mounted in contact with the back of the substrate via a hole ultrasonically drilled in the alumina supporting platform. This technique was used initially in order to calibrate the substrate heating power supply. Temperatures of the source and substrate above this were measured by a total radiation pyrometer corrected for silicon emissivity [83] and for the absorption of the pyrex windows in the vacuum system. This absorption was determined by taking temperature measurements of a light filament through an open part in the vacuum system and then through the pyrex window. Good agreement in the overlap temperature range of 750°C to 950°C was found between the two techniques.



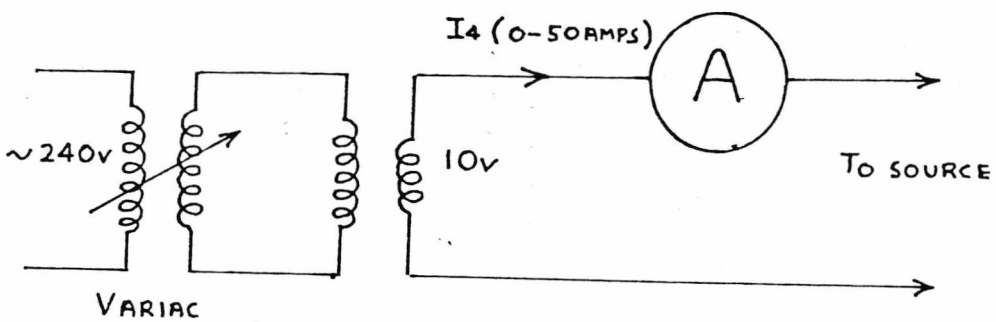


FIGURE 4.6 : METAL EVAPORATION SOURCE AND POWER SUPPLY

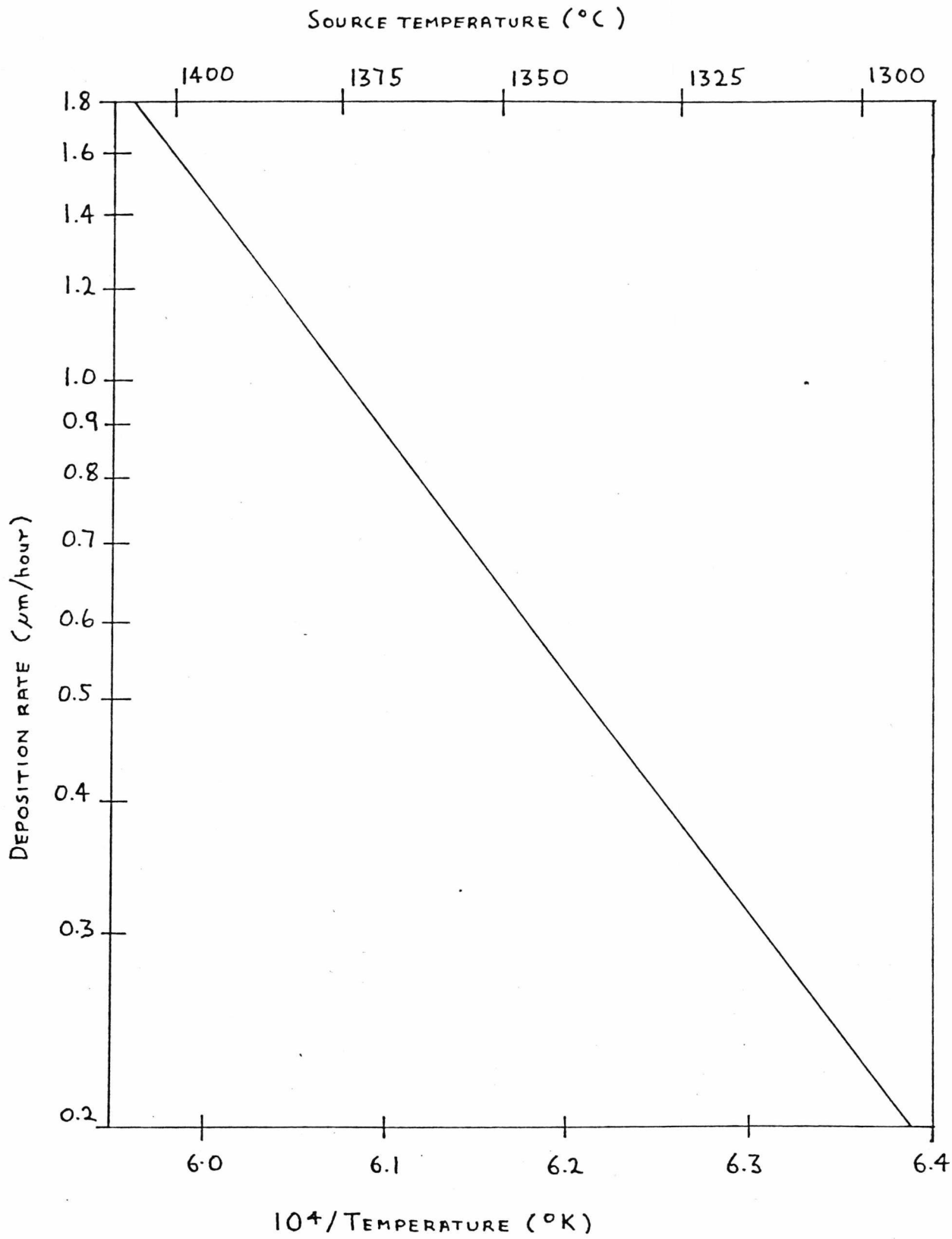


FIGURE 4.7 : VARIATION OF SILICON DEPOSITION RATE ON THE SUBSTRATE WITH SOURCE TEMPERATURE.

Initially the silicon sublimation source emits impurities in a far greater concentration than in the bulk silicon. However, after a period of time the impurity concentration in the vapour stream will reduce to a value near that of the original bulk value. This variation being dependent on the dopant type being considered. However, after the order of 1 μm of the source has been sublimed the impurity concentration will stabilise and this is then termed an 'equilibrium' source. In all cases equilibrium sources were used in this work, and it has been shown[71] that using such a source will lead to a grown layer of negligible variation in impurity concentration. The impurity profile of the grown layer considering the source material used during this work is shown in figure 4.8. This indicates the profile obtained from using a non-saturated source which was obtained from the work of Parish[71]. This gives the required information as to the impurity concentration in the grown layers when an equilibrium source is being used. From the profiling techniques used by Parish[71] this value of impurity concentration can be taken to an accuracy of about ±4%. The work of Parish[71] should be referred to for a detailed analysis of this mechanism. The techniques employed during this present work for the growth of epitaxial layers have been well experimentally verified to give good quality layers[36,71]. Layer thicknesses of up to the order of 5 μm were grown in order to ensure that punch-through conditions would not occur during the characterisation of the final devices.

4.6. FORMATION OF THE INTERFACES

All the silicon substrates used in this work were given the following chemical treatment before being placed in the U.H.V. system.

(I) Ultrasonic rinse in methanol for 5 minutes in order to remove any grease or soluble deposit.

(II) Blow dry the substrate with an air jet.

(III) Immerse in HF for one hour in order to remove surface oxide

(IV) Decant most of the HF and dilute with methanol.

(V) Decant most of the resulting mixture and dilute with methanol.

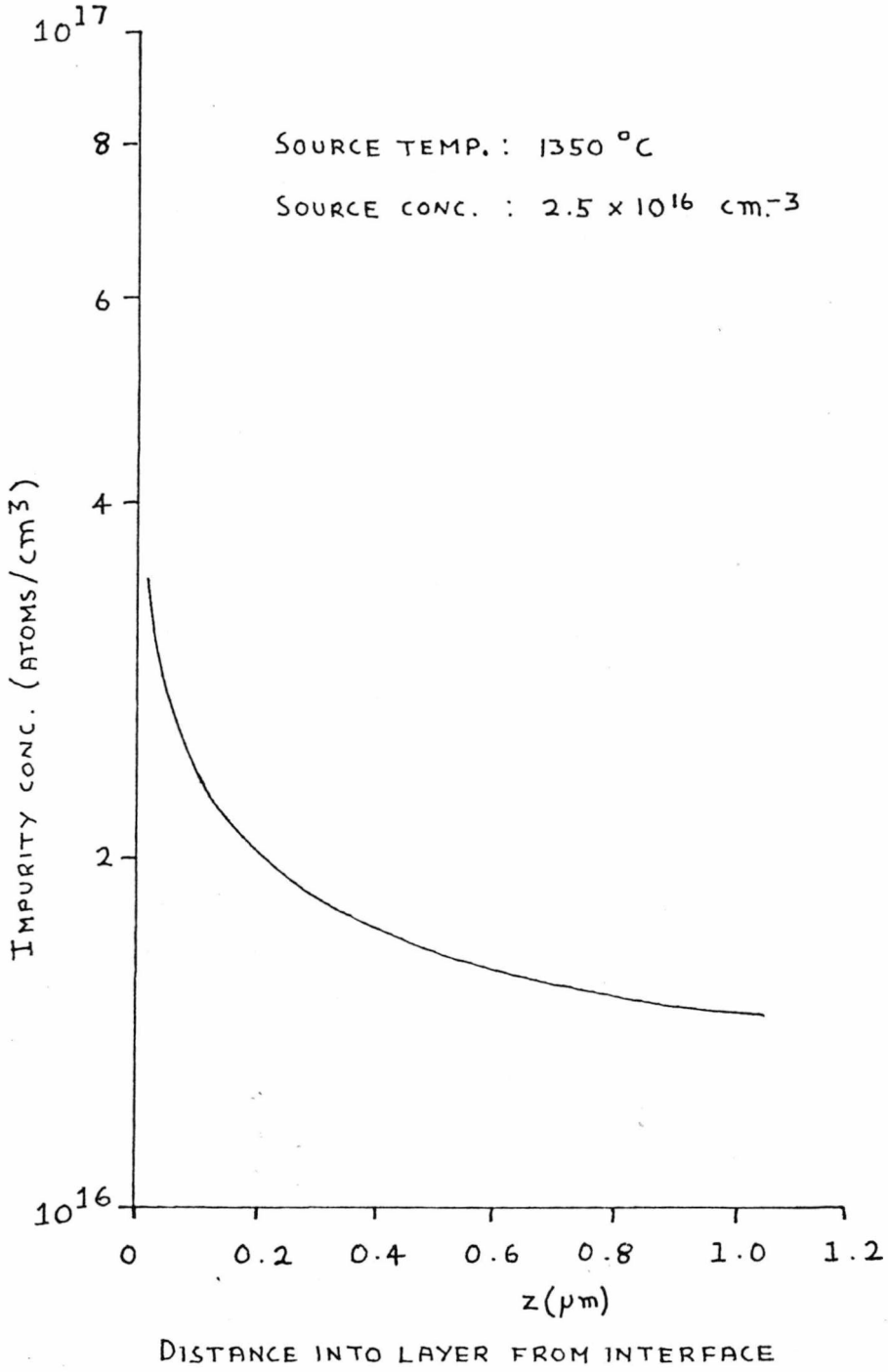


FIGURE 4.8 : EPITAXIAL LAYER IMPURITY PROFILE FOR NON EQUILIBRIUM SOURCE

(VI) While spraying with methanol transfer the substrate to pure methanol.

(VII) Leave immersed in methanol until required, to prevent the growth of surface oxide.

Methanol was used for this purpose as it has been found[36] that the use of acetone, ether, isoproponal or triklone will result in residual stains which the heat cleaning treatment will not remove. Deionised water has also been found to leave residual stains. When required the substrate was removed from the methonol and immediately connected via the four silicon blocks to the tantalum clips on the holder/heater assembly. The rotary motion drive was then quickly located in the vacuum chamber and the pump down sequence commenced.

After the system had been pumped down and baked out, and also all the electrical system components throughly outgassed, the following procedure was adopted for the formation of the interfaces.

(I) The substrate surface was cleaned by heating to 1200°C for 5 minutes and then the temperature reduce to the value required. This procedure was carried out when the substrate was in a shielded position to prevent any unwanted contamination.

The next three stages relate to the growth of an epitaxial layer.

(II) The source was set to the required sublimation temperature.

(III) The substrate was then moved (on the rotary drive) to the deposition location.

(IV) After the required thickness of layer had been grown the deposition was terminated by returning the substrate to its original position behind the shield. The substrate and source current supplies were then turned off.

The following stages apply to both interface formation techniques.

(V) Sufficient current was passed through the metal evaporation source in order to evaporate the metal being used.

(VI) The substrate was located above the metal evaporation source and the metal film deposited on the clean silicon surface.

(VII) The metallisation was terminated by returning the substrate to its original position and turning off the current supply to the source.

The above procedure was that generally adopted and was found to give consistent and reproducible results for all the metals used.

The U.H.V. system could then be brought up to atmospheric pressure by the use of dry nitrogen and the substrate removed from the holder/heaterassembly.

4.7. SURFACE ASSESSMENT

Optical microscopy was used as the first method of assessment of the silicon surface condition. This was then followed by electron microscope studies of the silicon surface at various stages during the experimental procedure. Initially the substrate surface was examined after the chemical cleaning process and no unwanted chemically induced surface defects could be observed. Several substrates were examined after the heat cleaning process at 1200°C and this revealed an almost featureless surface under the electron microscope with no evidence of any thermally induced surface defects. Also at this stage, as mentioned in chapter 3, the surface of the heat cleaned substrates were thermally probed in order to detect any evidence of the formulation of a P-type layer. This involves the contacting of a heated probe and a room temperature probe to the surface under investigation. A Seebeck voltage is produced whose polarity indicates whether the charge carriers are holes or electrons. No p-type layer could be detected on any of the surfaces examined and several substrate surfaces were tested in this manner having been heated for far longer than 5 minutes and also at higher temperature than 1200°C. An electron microscope study was carried out on several epitaxial layers grown in the U.H.V. system, again an almost featureless surface was observed. The discernable features probably outlines the lateral spreading of the growth centres[67] which would indicate that the required two-dimensional nucleation was occuring.

The crystallinity of the silicon epitaxial layer could be examined by the use of a preferential etch which etchs slower in the (111) direction than in other directions and thus exposes the (111) planes. A 20% solution of NaOH at about 60°C [84] was used for this purpose. A surface near to a (111) plane etched in

such a solution for a few minutes produces small flat bottomed triangular etch pits in the surface and this effect can be examined under the microscope to indicate the extent of the crystaline perfection. Regions of poor crystallinity were usually found in the epitaxial layer close to the position of the substrate contacts probably because of an insufficient heat treatment caused by the contact acting as a heat sink. However, these areas were avoided when the actual devices were formed.

Perhaps the most important defect to be examined are stacking faults[35] because, as mentioned in chapter 3, these are mainly caused by substrate surface contamination, and this is especially important as we are trying to achieve a clean silicon surface. An optical microscope can be used to detect stacking faults, chemical etching (with the Sirtl etch[35]) being necessary to make the faults visable. Using the sublimation techniques mentioned the stacking fault density was less than $10^2/cm^2$.

Thus from the observations on the heat cleaned surfaces and also the epitaxial layers grown on the surfaces it would appear that the heat cleaning technique does produce a clean silicon surface.

CHAPTER 5

MEASUREMENT TECHNIQUES

5.1. FABRICATION OF THE DEVICES

Initially the silicon substrates, with the evaporated metal film, were given an ultrasonic wash in methanol in order to remove any solu ble deposits that may have formed after the substrate was removed from the vacuum chamber. Particularly due to the actual dimensions of the silicon substrates used, a technique of depositing small drops of black wax onto the metal surface was employed in order to form the etch mask for the actual devices. It was possible to form a four by two array of dots on the metal surface, avoiding the area close to where the current feed contacts were made onto the substrate. This dotting process was achieved by placing the substrate onto a hot plate which was maintained at a temperature of approximately 80°C . A small spheroid of black wax supported by a thin wire was then lowered onto the surface of the metal, with the aid of a micro manipulator, the wire then being raised after a suitable dot had been formed. By careful practice it was possible to use this technique in order to produce well defined dots of wax on the metal surface with diameters of 0.5mm to 2mm depending on the duration that the wax spheroid was in contact with the metal surface. After the array had been completed the substrate was allowed to cool and then the unwanted metal film removed by immersion in a suitable etch. The etches used for the various metals are listed in Appendix B. The black wax could then be removed by an ultrasonic wash in triklone, and finally the substrate was given a rinse in methanol and thenblow dried. The size and shape of the dots produced in this manner could be determined from optical microscope photographs. Thus the area could be calculated to an accuracy of about $\pm 1\%$. This process was found to consistently produce good quality, well defined metal dots on the substrate surface, as well as being a very quick and relatively easy technique to perform. As mentioned in Chapter 2, this technique has one advantage over the production of the dot array in the U.H.V. chamber, in the sense that the uncertainty of contamination from a metal mask is avoided.

5.2. INITIAL PROBE MEASUREMENTS

Room temperature probing of the devices, in order to determine their I-V characteristics, was initially performed in order to obtain some immediate information with regards to the rectification properties of the device produced. The measurements were achieved by mounting the substrate onto a copper platform which had been given a roughened finish. A Ga/In eutectic was employed in order to ensure a good ohmic back contact. The probe used consisted of a thin gold wire with a spheroid formed at the end by the use of a welding torch. The gold wire was mounted in a fine capilliary bore glass tube, which had been heated and tap ered at one end in order to provide a good seating for the gold spheroid. The glass tube was then mounted via a sliding fit into a micro-manipulator in order that a reproducible and consistent pressure could be obtained onto the metal contact. Basic I-V characteristics were obtained by connecting the probe head to a curve tracer. Typical results obtained for the metal-silicon contacts, formed on the heat cleaned surfaces are shown in figures 5.1. and 5.2. These graphs were drawn from polaroid shots taken from the curve tracer. As can bee seen from the plots, these initial measurements gave a very good idea into the variation of the I-V characteristics with the various metals used. This initial test was also useful in that any doubtful devices could be eliminated before the more detailed characterisation of the devices was undertaken. Also these rough I-V plots provided a base for determining the most useful temperature range to be investigated for each type of metal-silicon contacts.

5.3. I-V MEASUREMENT EQUIPMENT AND PROCEDURE

Detailed I-V characterisation of the devices was performed under varying temperature conditions. This was achieved by the use of an Oxford DN70 cryostat in conjunction with a DTC2 temperature controller. The measurement equipment used was a Keithley G10CR electrometer and Solartron A200 digital voltmeter. A basic diagram of the measurement setup is shown in figure 5.3. RV_1 and RV_2 providing a course and fine adjustment to the bias voltage with S1 providing the facility for both forward and reverse characteristics to be easily obtained. A good single earth point was maintained in order to eliminate any possible earth loops, especially when considering the magnitude of currents to be measured.

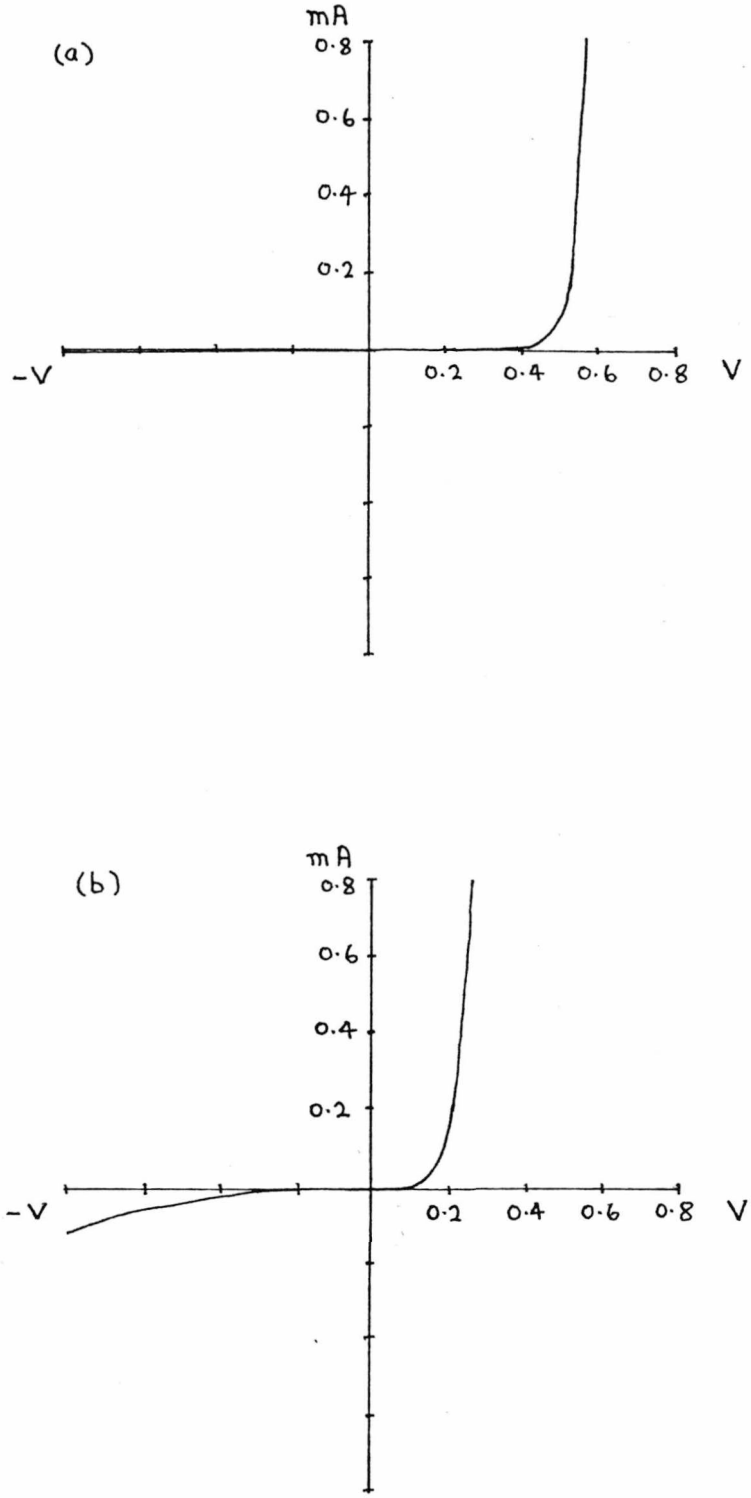


FIGURE 5:1 : INITIAL I-V CURVES FOR (a) Au AND (b) Cr

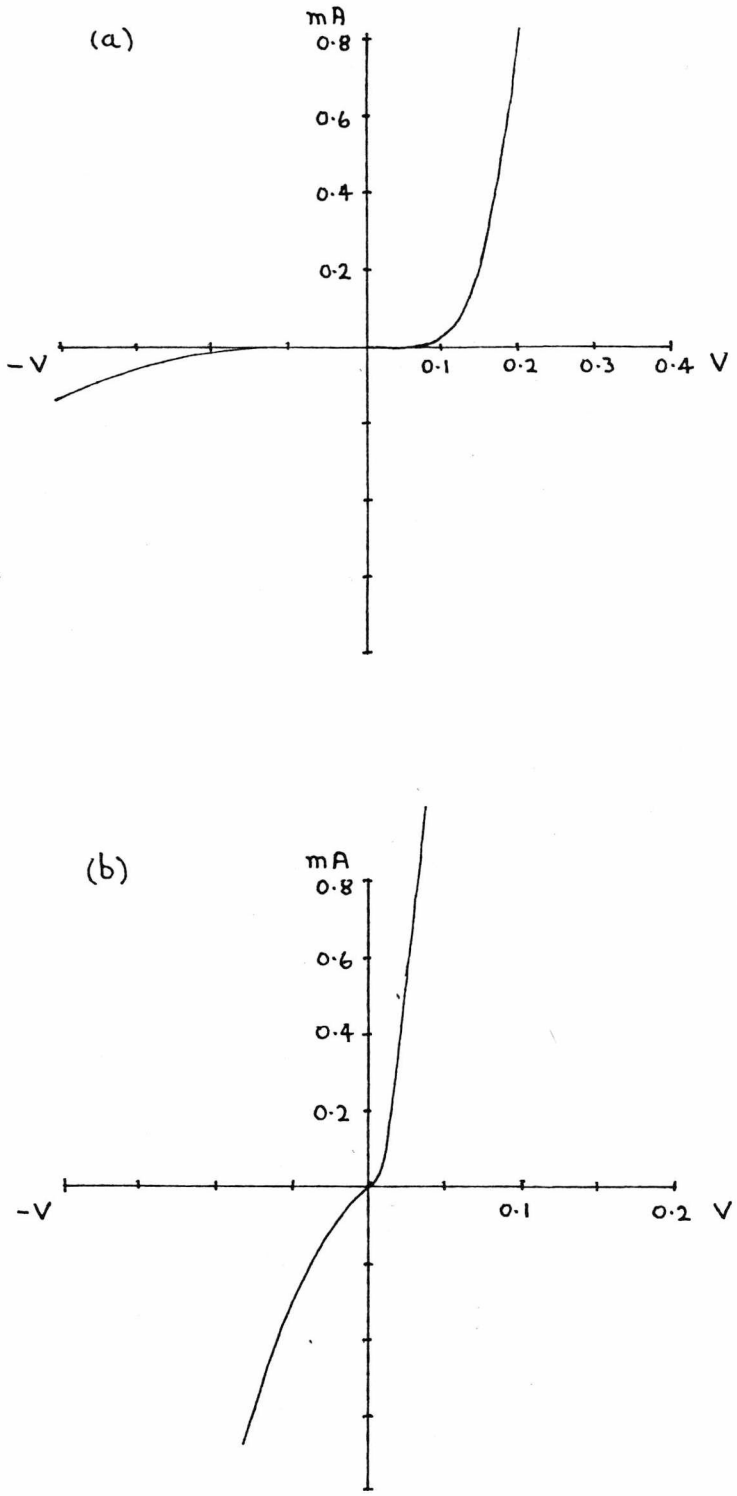


FIGURE 5.2 : INITIAL I-V CURVES FOR (a) Ag AND (b) Al.

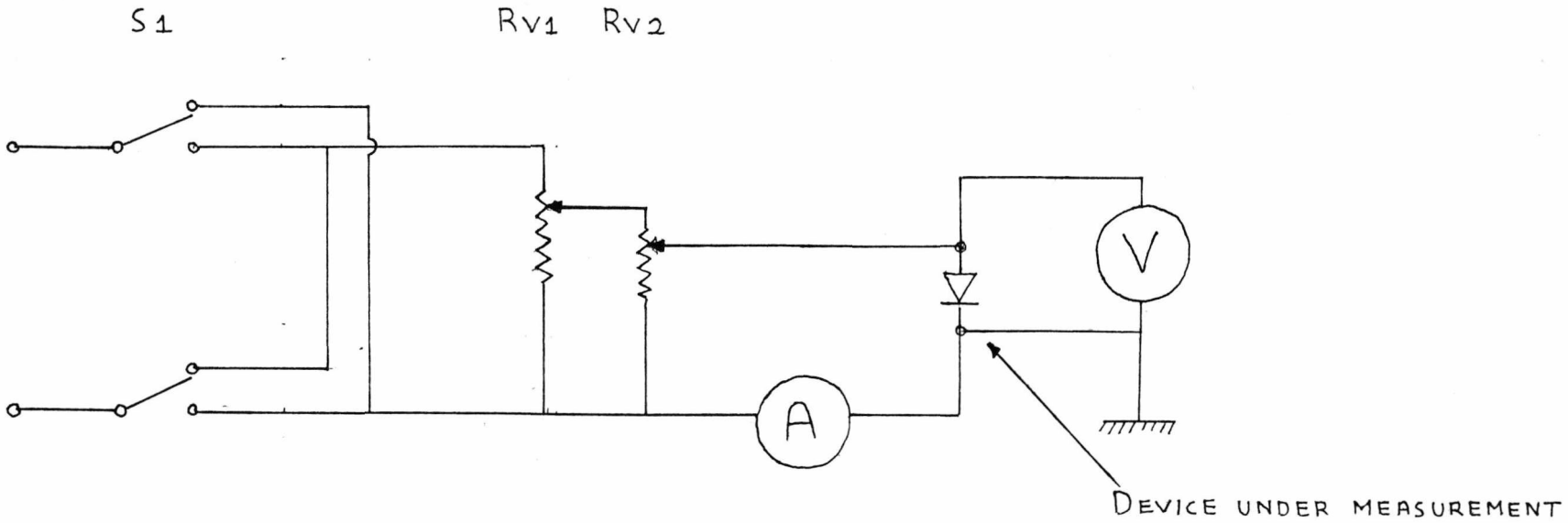


FIGURE 5.3 : I-V MEASUREMENT SET-UP.

All the bias circuitry was mounted in a screened box with co-ax cables being using externally right up to the probe head. Figure 5.4. indicates a crossection of the DN70 cryostat. The sample mounting area of the cryostat was modified in order to suit the devices fabricated during this work. A probe head was manufactured in order to make contact onto the particular device required for measurement. Figure 5.5. shows a crossection through the probe head and sample mounting area. As in the initial probe measurements a Ga/In eutectic was employed in order to ensure a good ohmic back contact onto the gold plated sample mount, the gold spheroid on the probe head providing the electrical contact onto the metal dots. After the sample had been mounted in the cryostat, the system was pumped down to a pressure of 10^{-2} torr by the use of a rotary pump. Liquid nitrogen was then used in order to activate the sorption pump and to reduce the temperature of the device to less than 100°K. It was then possible, by the use of the temperature controller, to obtain I-V characteristics of the device over a wide range of temperatures with a temperature stability of the order of ± 0.5°K. Equal increments in reciprocal temperature steps were used over such a range as to produce the most useful and accurate readings. Errors in these measurements can be attributed to the relative impedance concerned with the various circuit elements and any stray effects especially as the magnitude of the measured current becomes very small. In general however results to an accuracy of less than $\pm 2\%$ should be possible.

5.4. I-V RESULTS

The following set of graphs are plots of log current versus voltage over the various temperature ranges investigated during this work. These consist of forward and reverse bias results for all four metals considered. Figures 5.6. to 5.13 are the results for the epitaxial layers and figures 5.13 to 5.21 the results for the heat cleaned surfaces. Several devices of each type were measured, and mainly due to the differing areas of the devices, the errors involved are considered in the interpretation of the results in chapter 6 rather than at this stage.

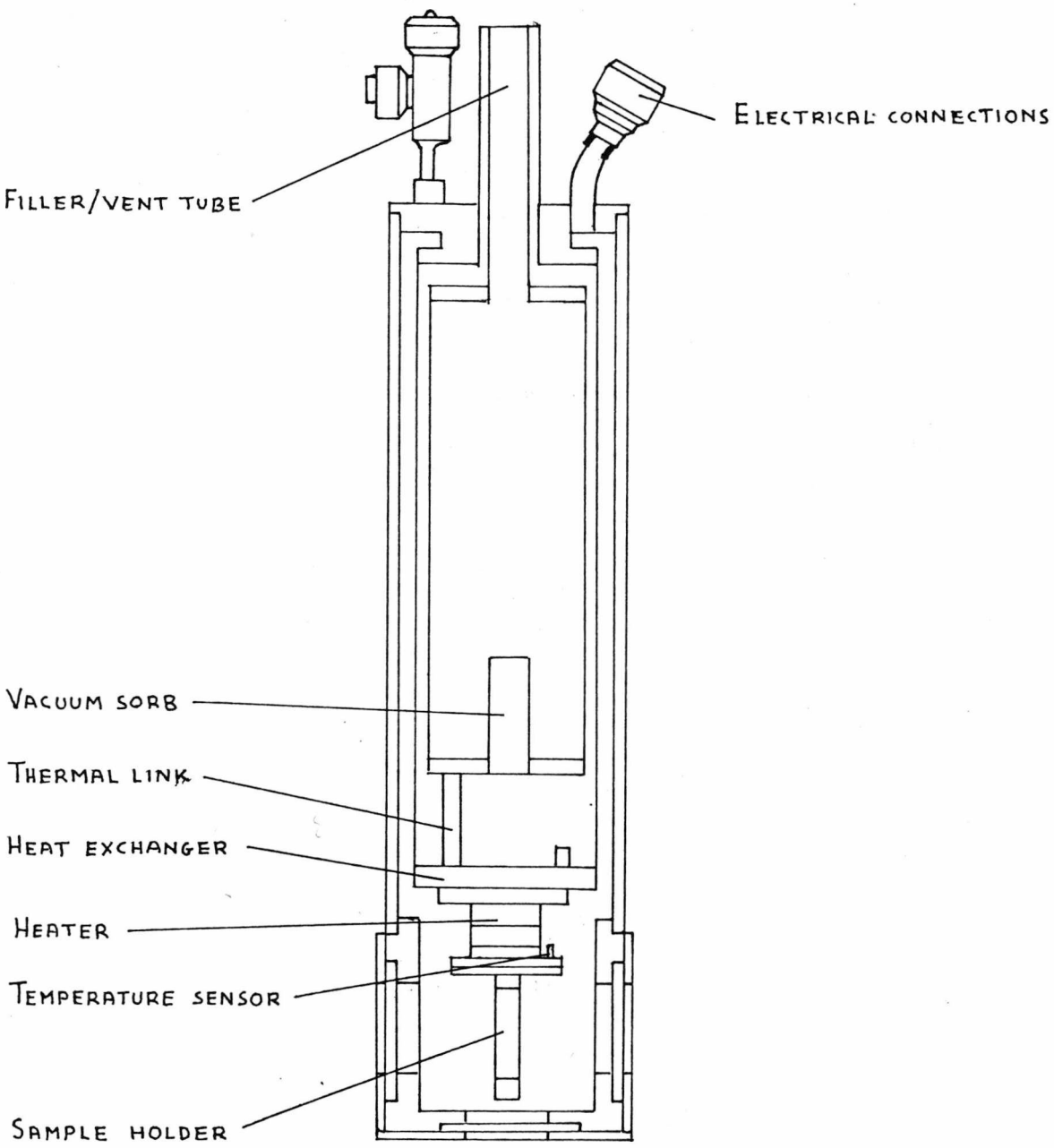


FIGURE 5.4 : CROSSECTION OF CRYOSTAT

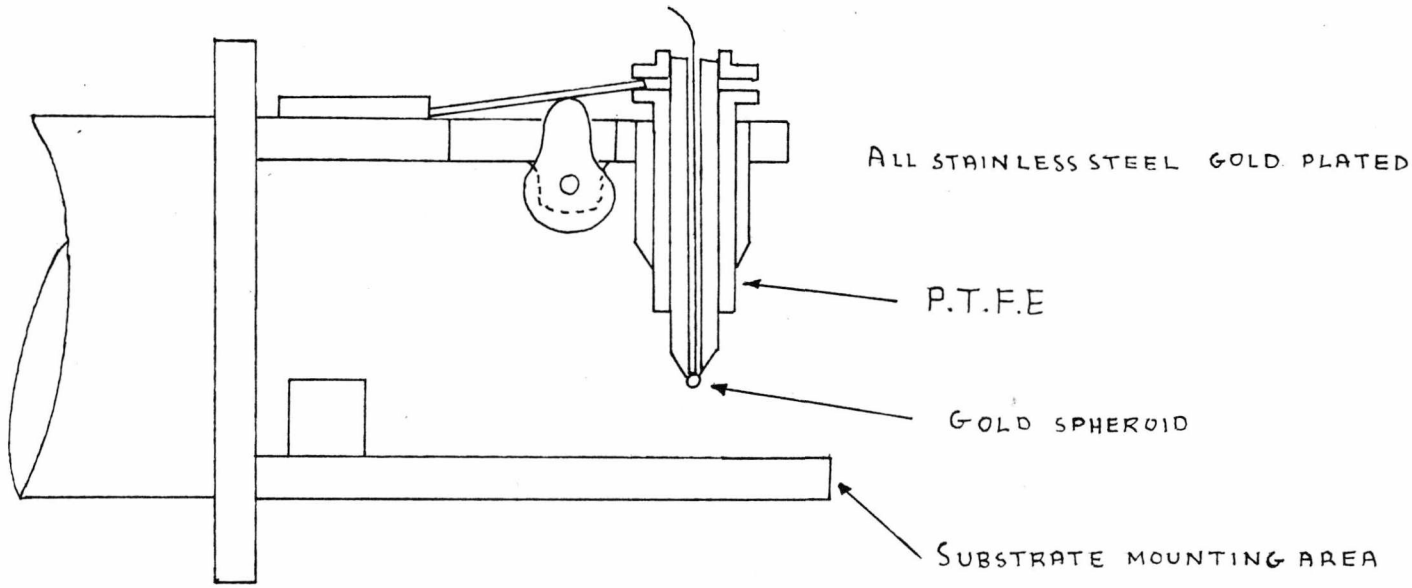


FIGURE 5.5 : CRYOSTAT PROBE HEAD

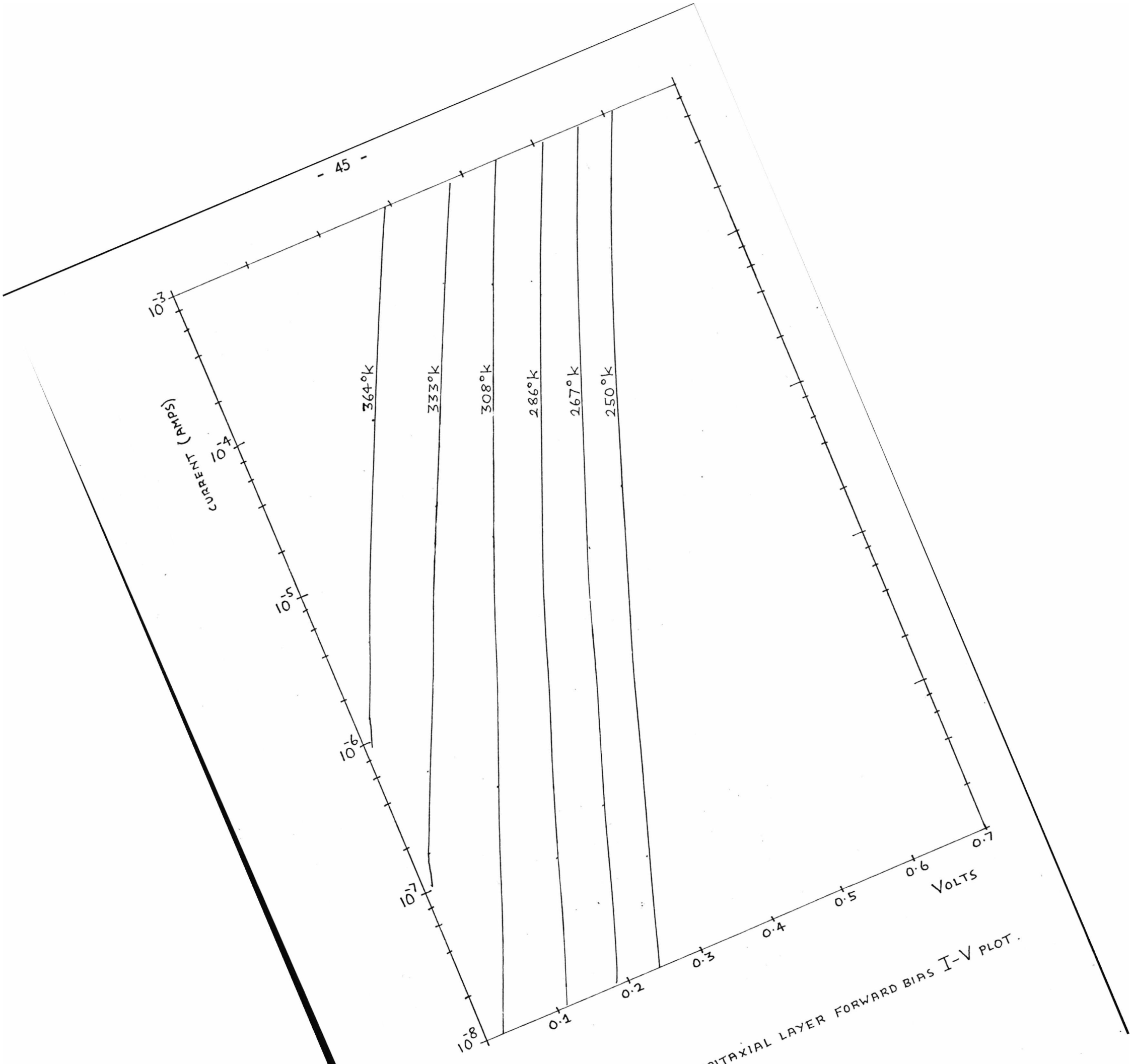


FIGURE 5.6 : Au- EPITAXIAL LAYER FORWARD BIAS I-V PLOT.

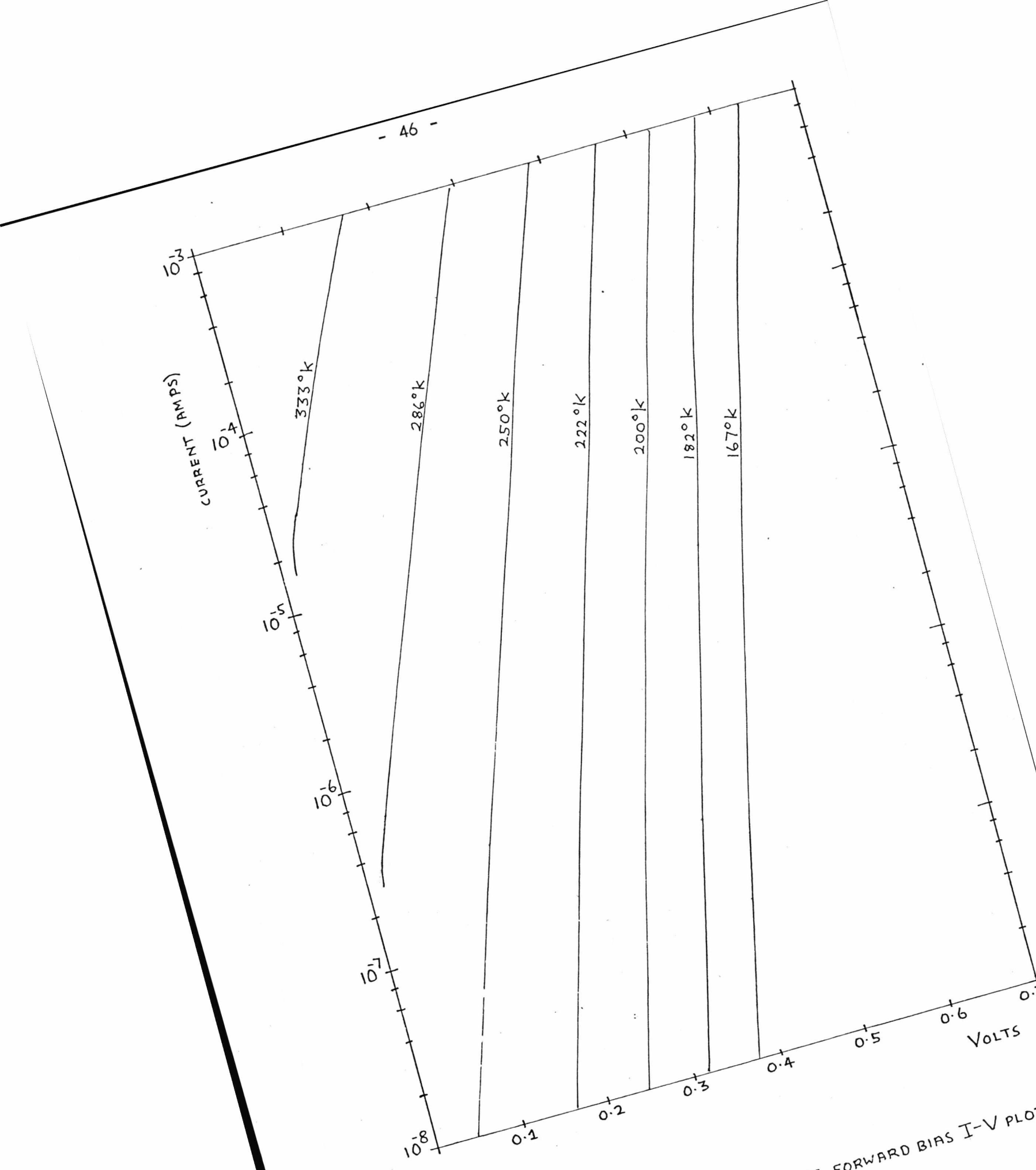


FIGURE 5.7 : Cr – EPITAXIAL LAYER FORWARD BIAS I-V PLOT.

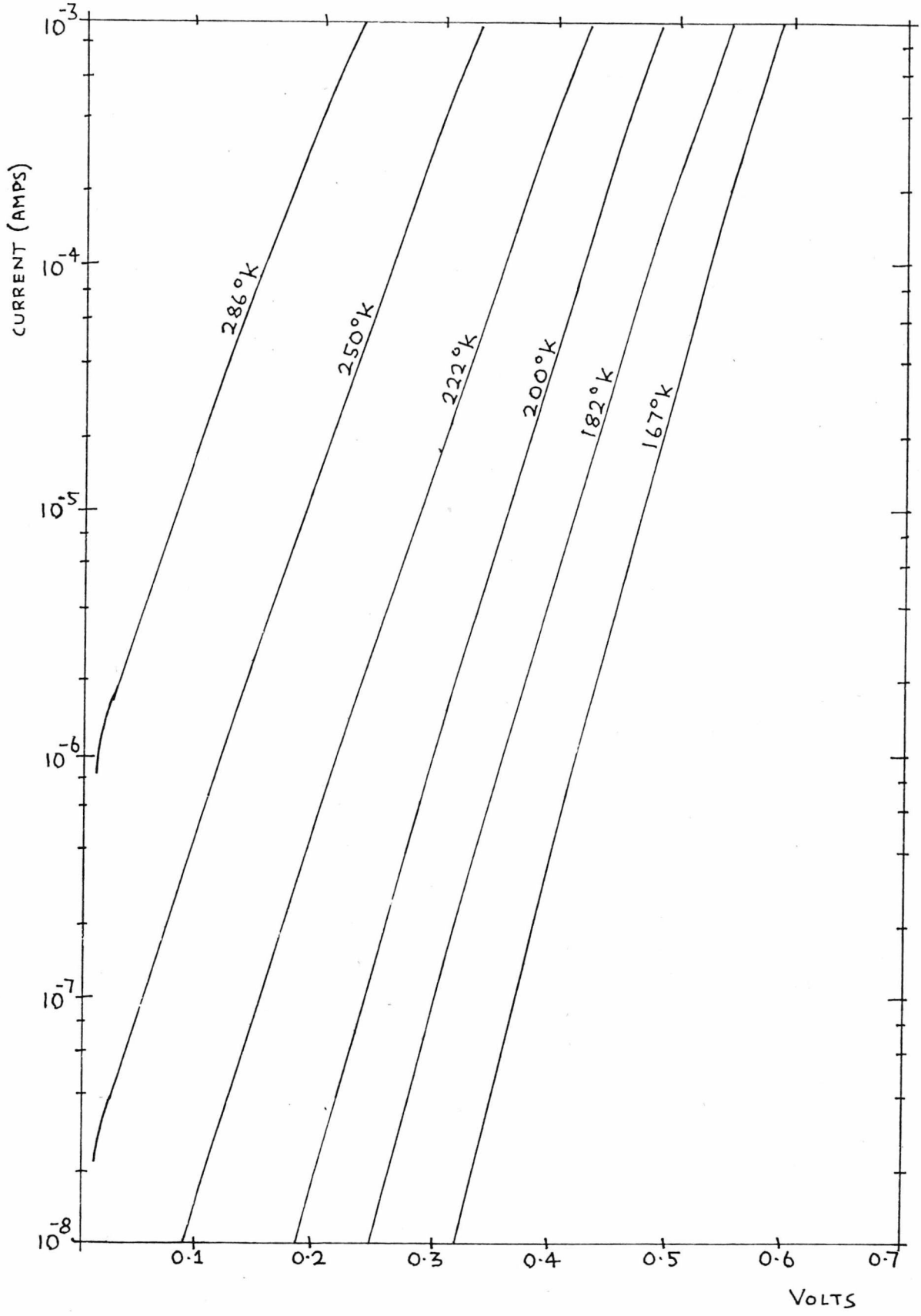


FIGURE 5.8 : Ag - EPITAXIAL LAYER FORWARD BIAS I-V PLOT

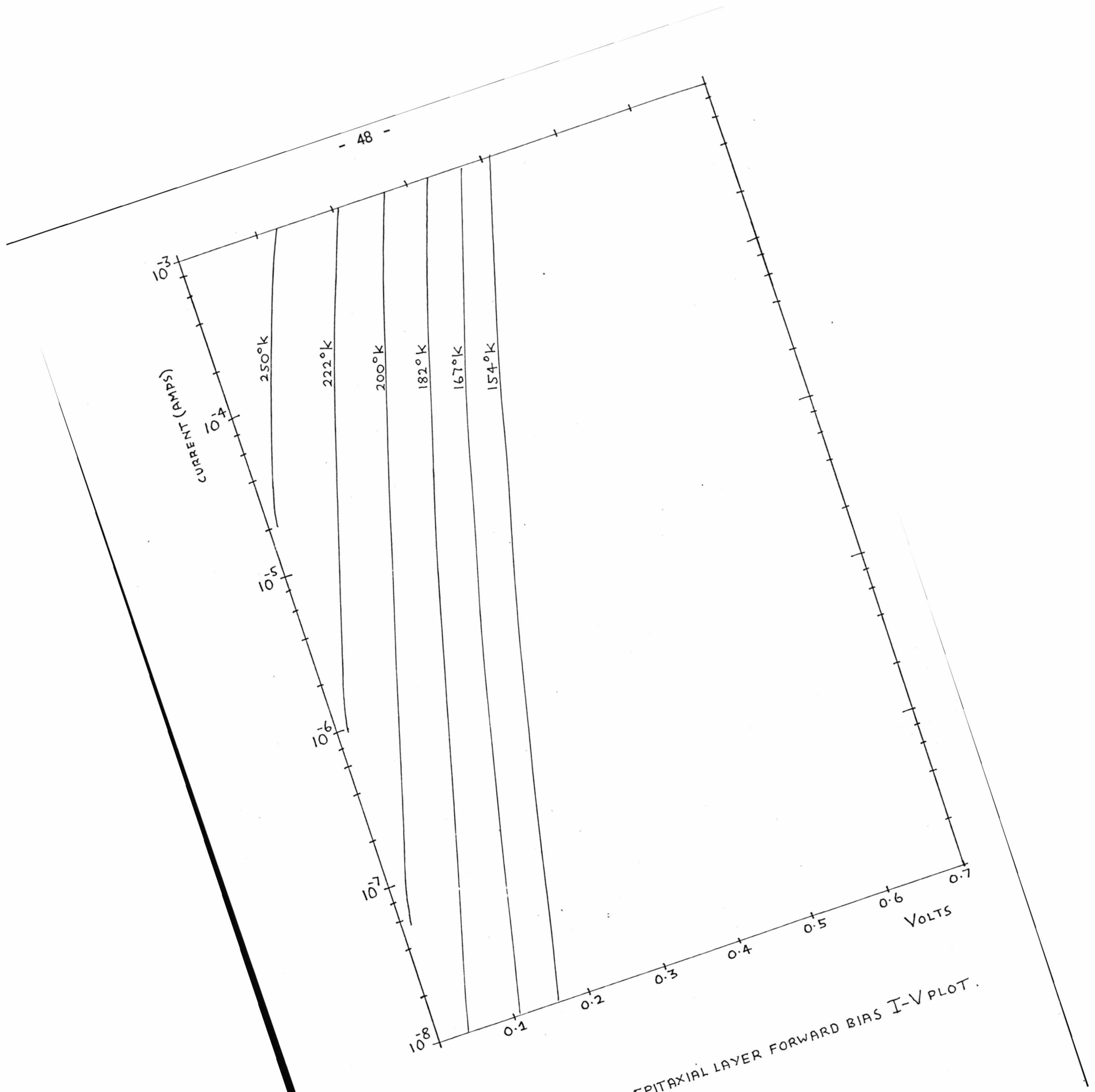


FIGURE 5.9 : Al - EPITAXIAL LAYER FORWARD BIAS I-V PLOT.

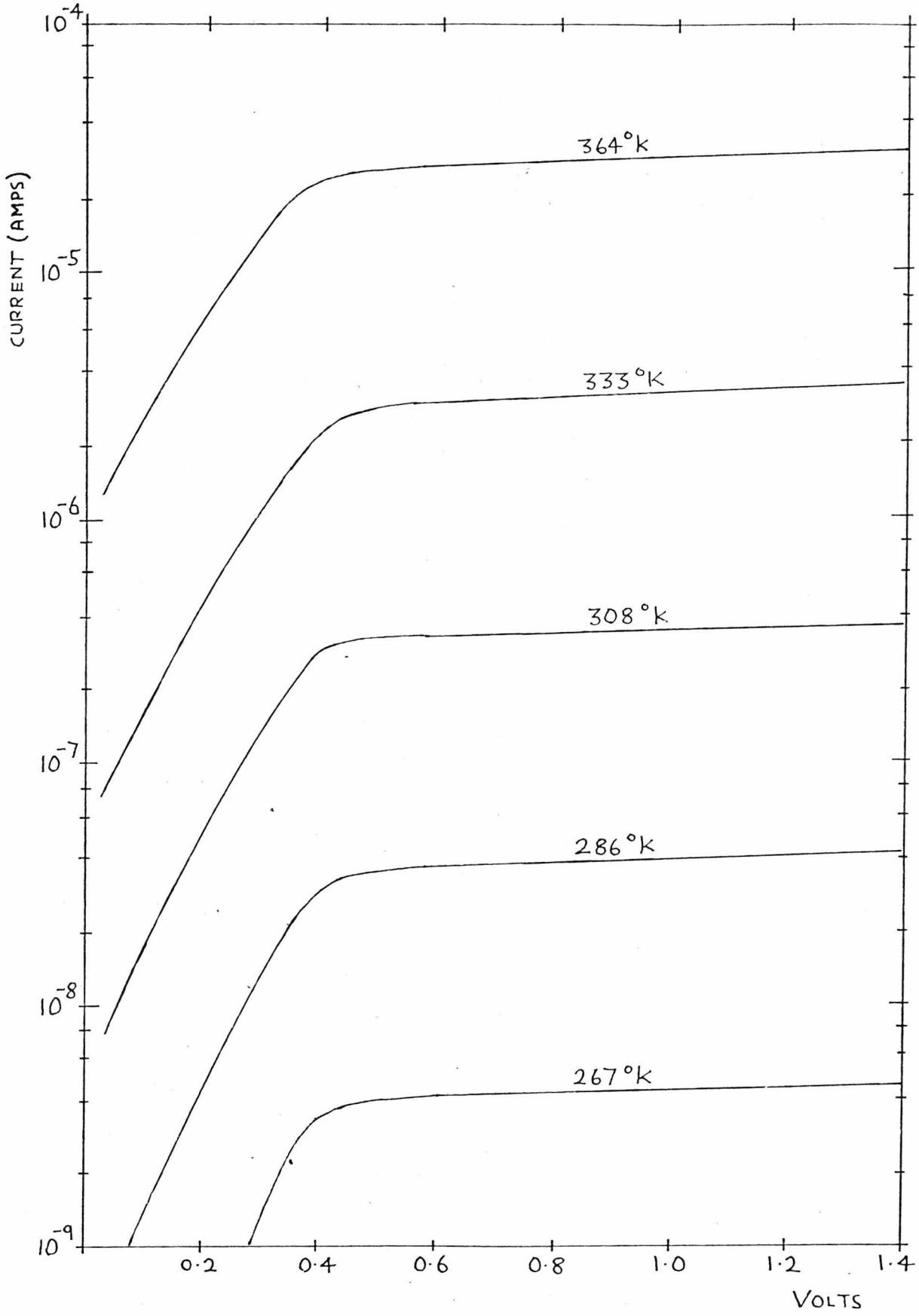


FIGURE 5.10 : Au- EPITAXIAL LAYER REVERSE BIAS I-V PLOT.

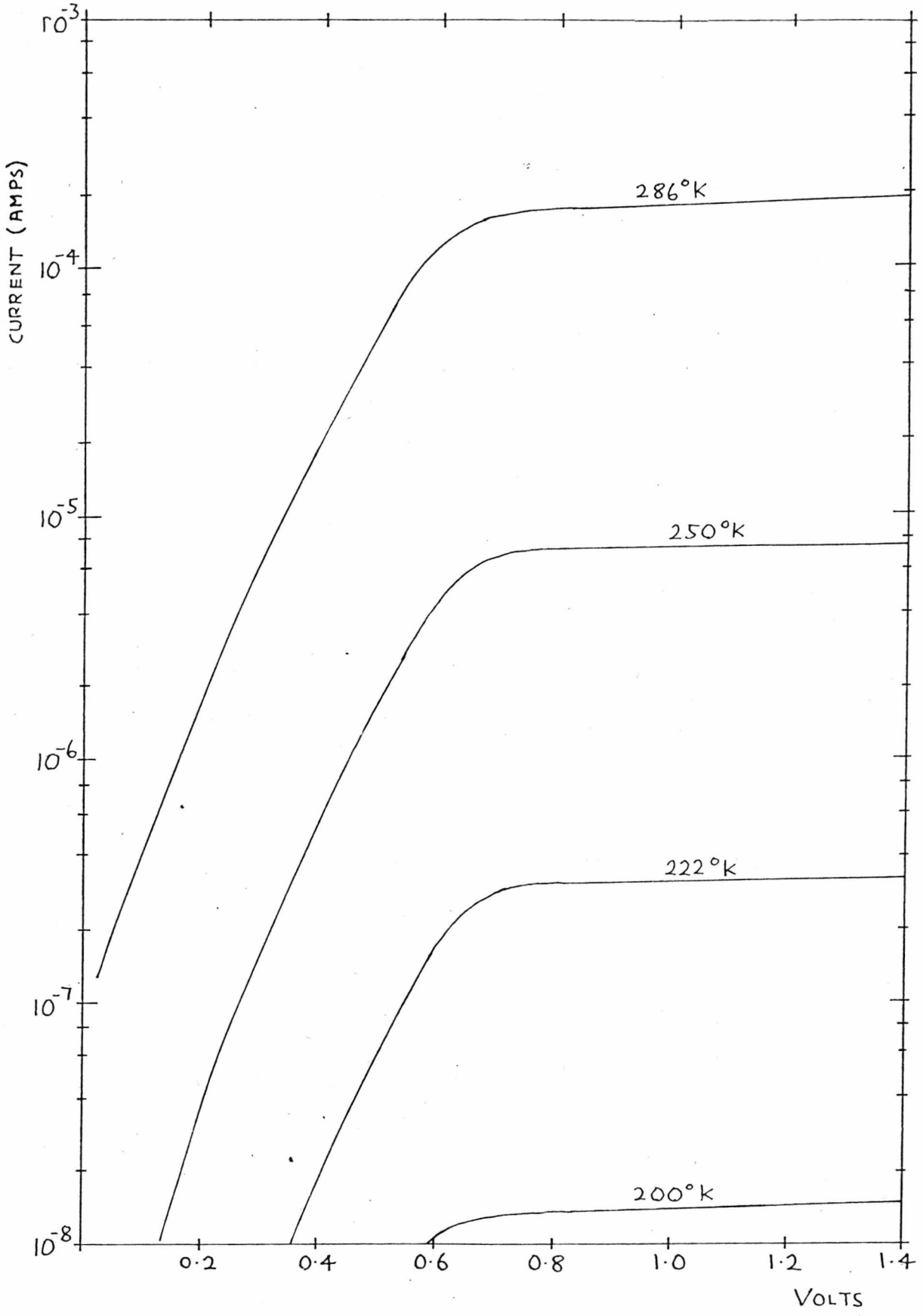


FIGURE 5.11 : Cr - EPITAXIAL LAYER REVERSE BIAS I-V PLOT

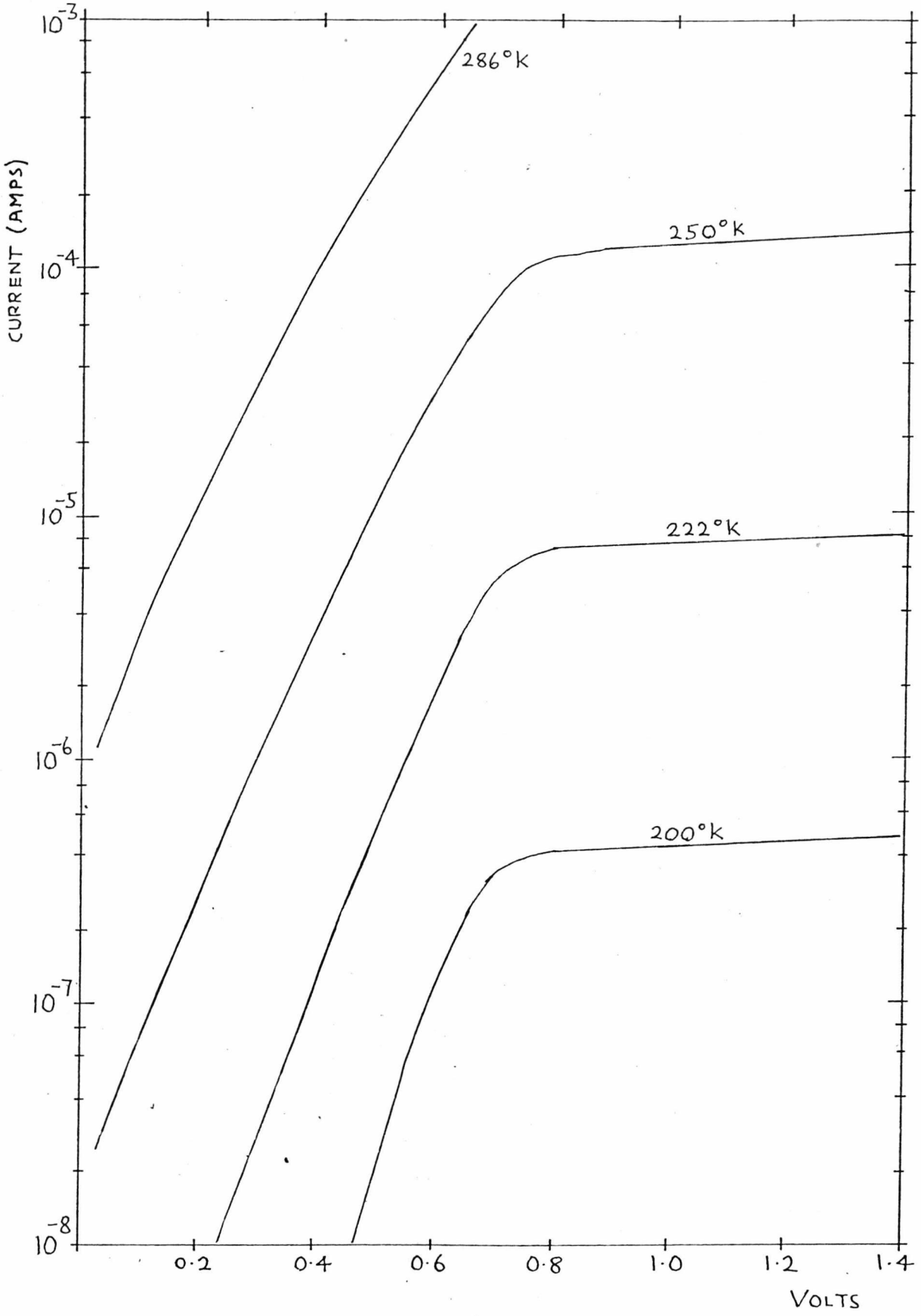


FIGURE 5.12 : Ag - EPITAXIAL LAYER REVERSE BIAS I-V PLOT

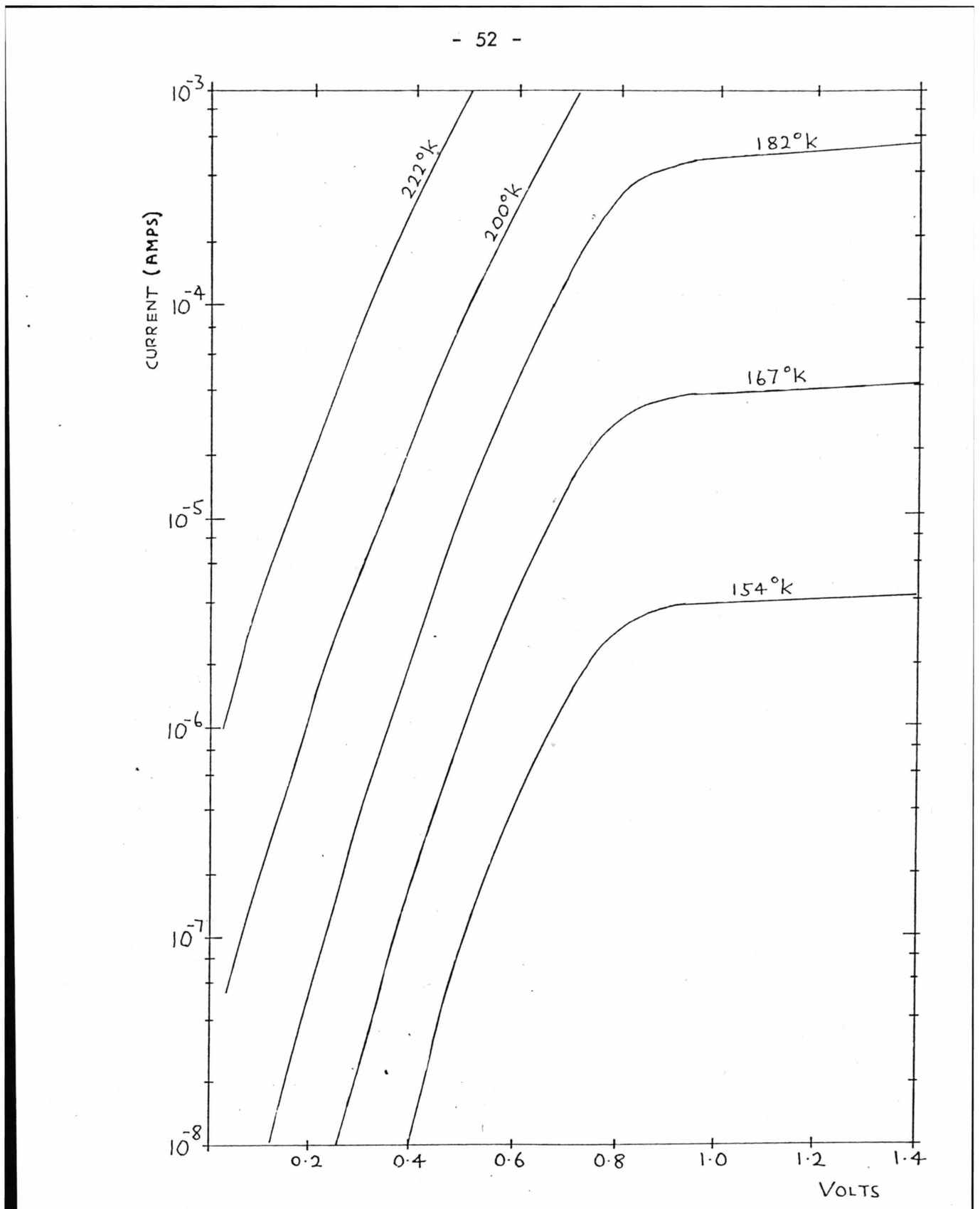


FIGURE 5.13 : Al-EPITAXIAL LAYER REVERSE BIAS I-V PLOT.

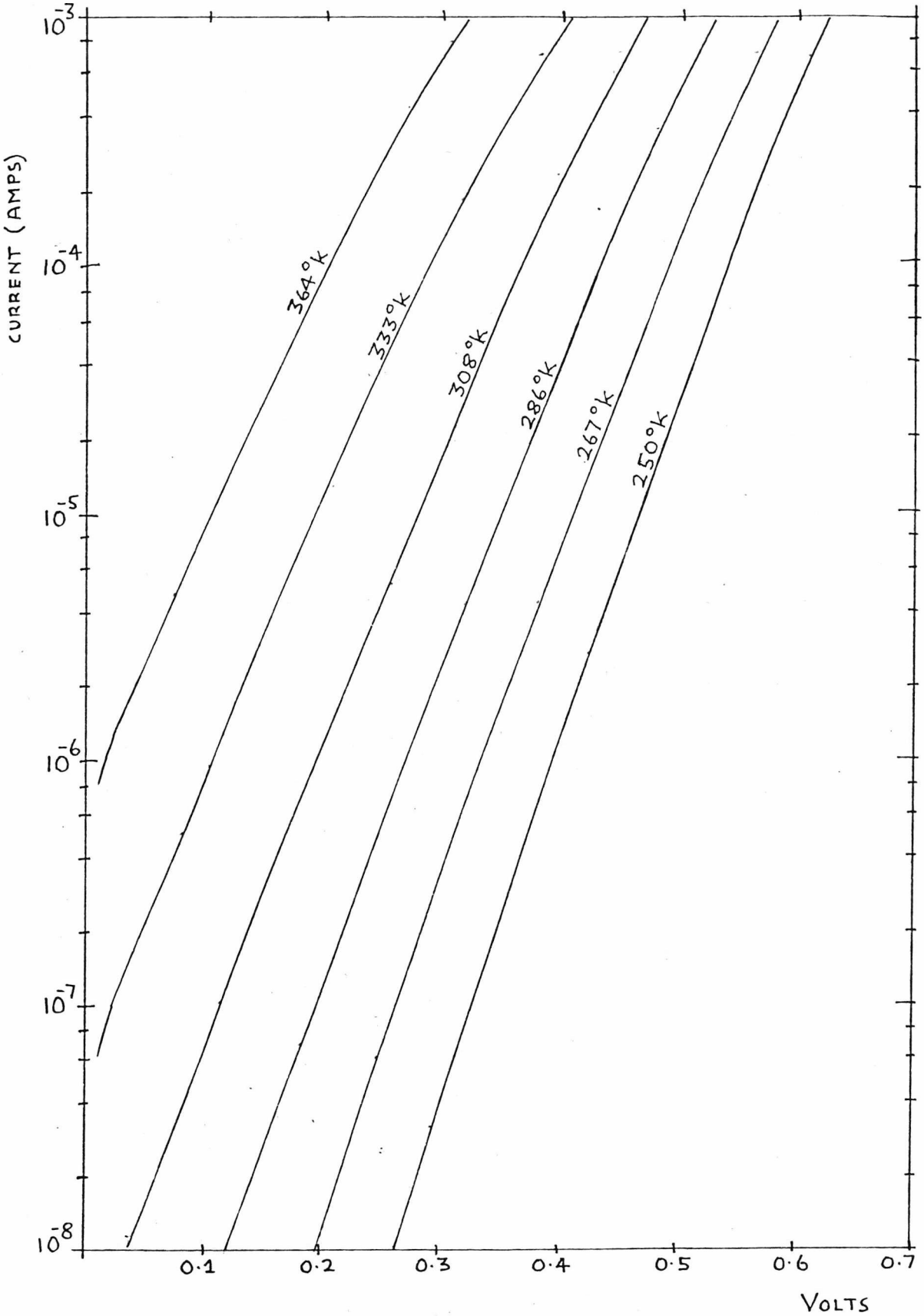


FIGURE 5.14 : Au-SILICON (HEAT CLEANED) FORWARD BIAS I-V PLOT.

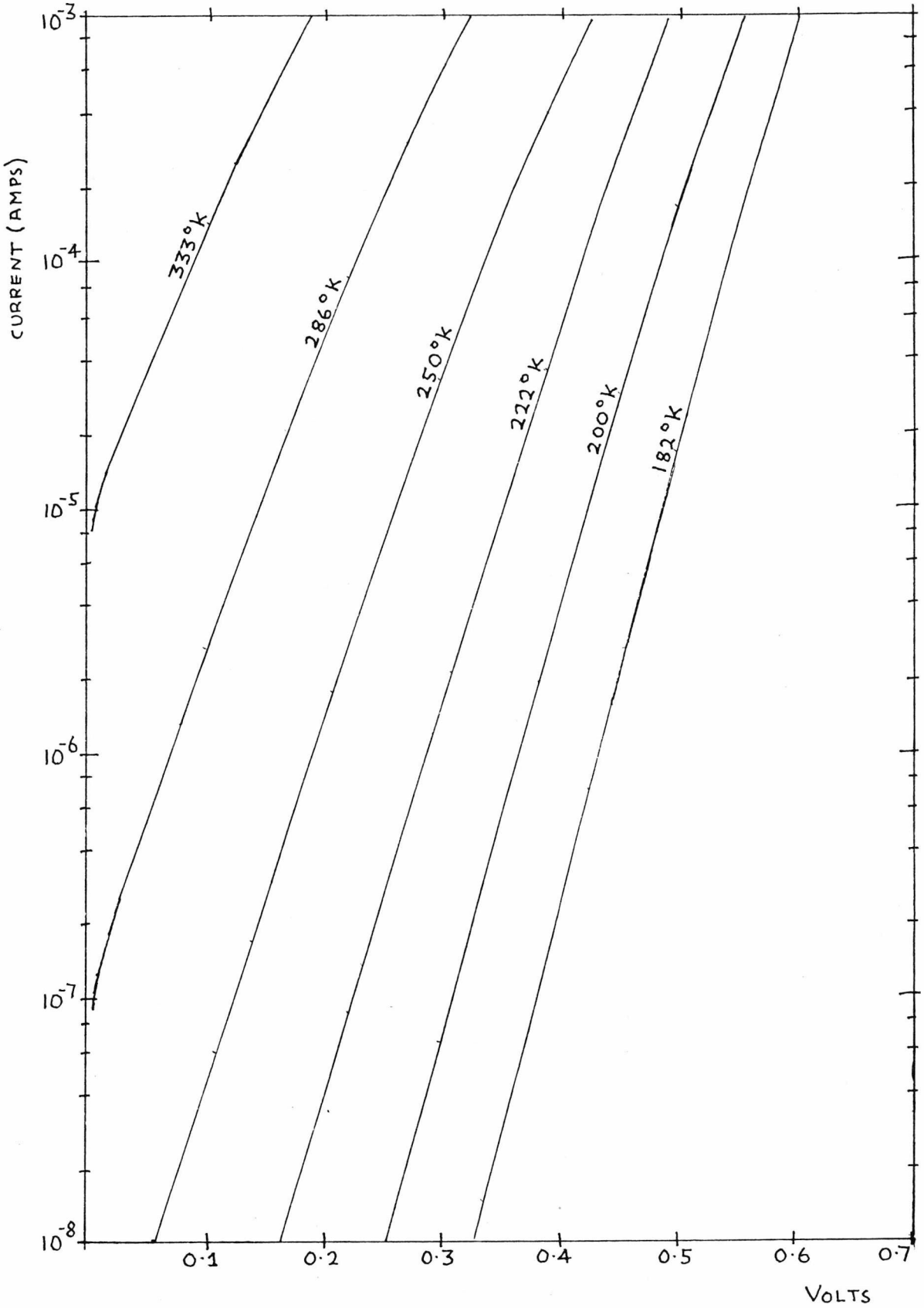


FIGURE 5.15 : Cr-SILICON (HEAT CLEANED) FORWARD BIAS I-V PLOT.

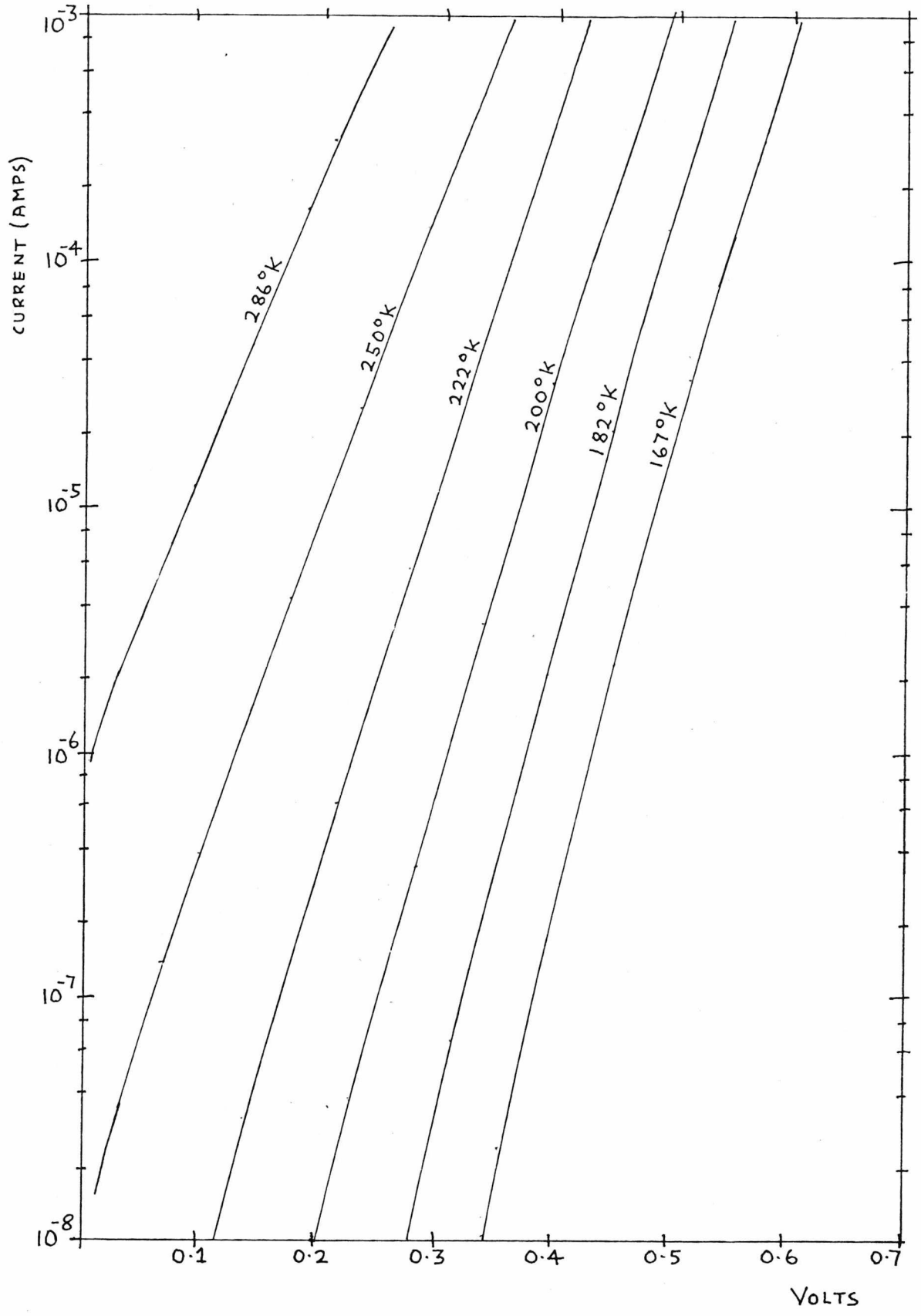


FIGURE 5.16: Ag-SILICON (HEAT CLEANED) FORWARD BIAS I-V PLOT.

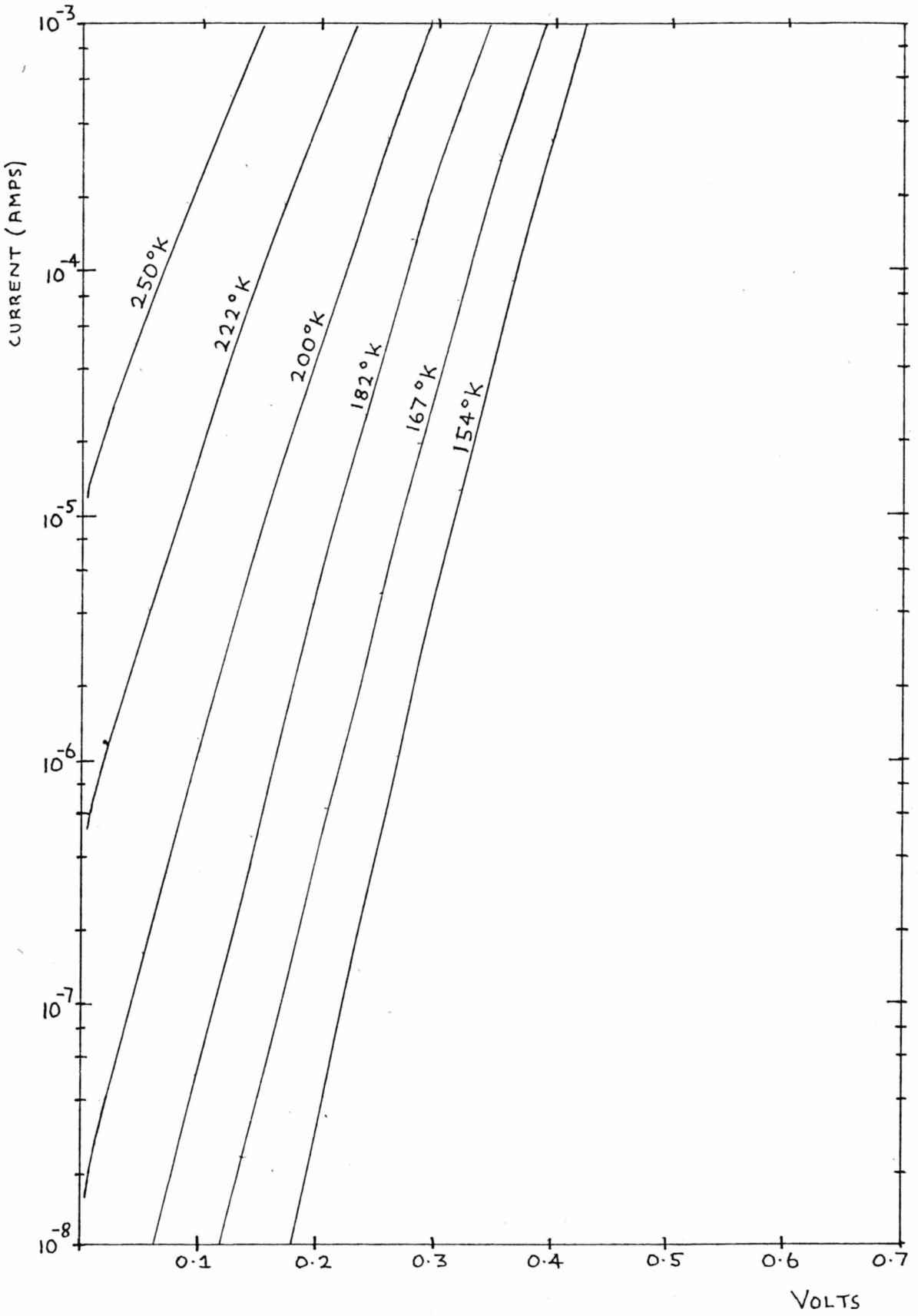


FIGURE 5.17 : Al - SILICON (HEAT CLEANED) FORWARD BIAS I-V PLOT.

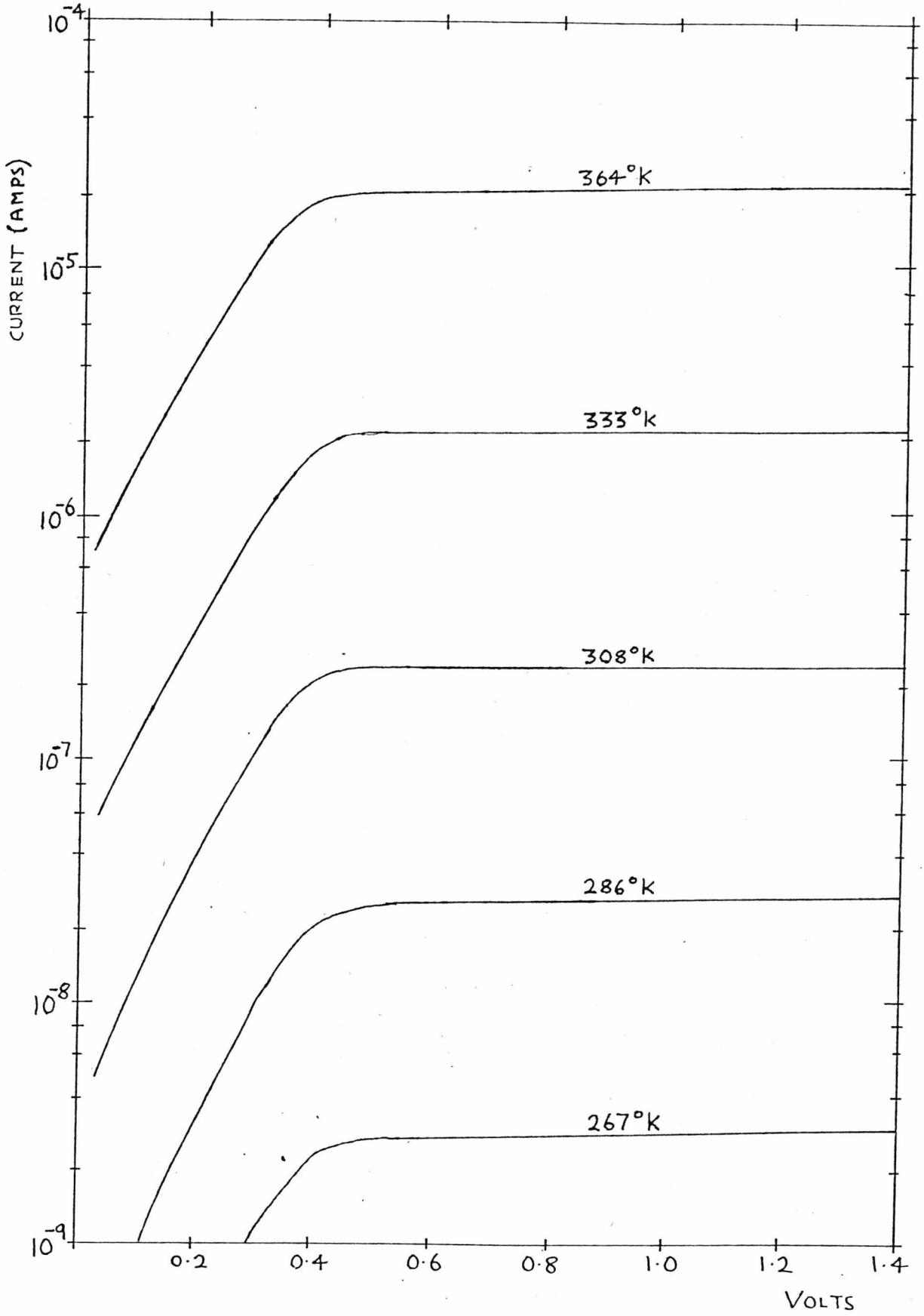


FIGURE 5.18 : AU-SILICON (HEAT CLEANED) REVERSE BIAS I-V PLOT.

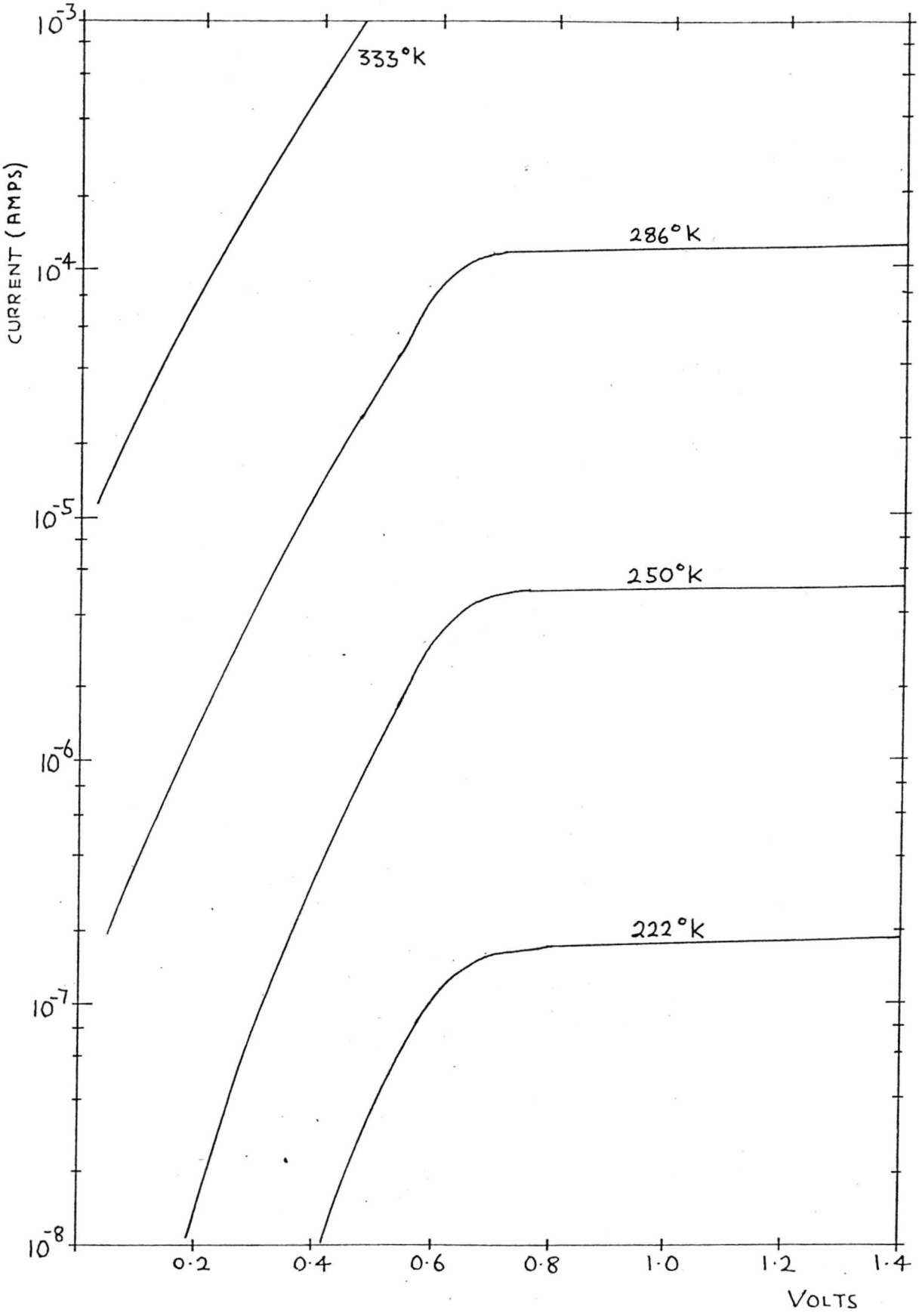


FIGURE 5.19 : Cr - SILICON (HEAT CLEANED) REVERSE BIAS I-V PLOT.

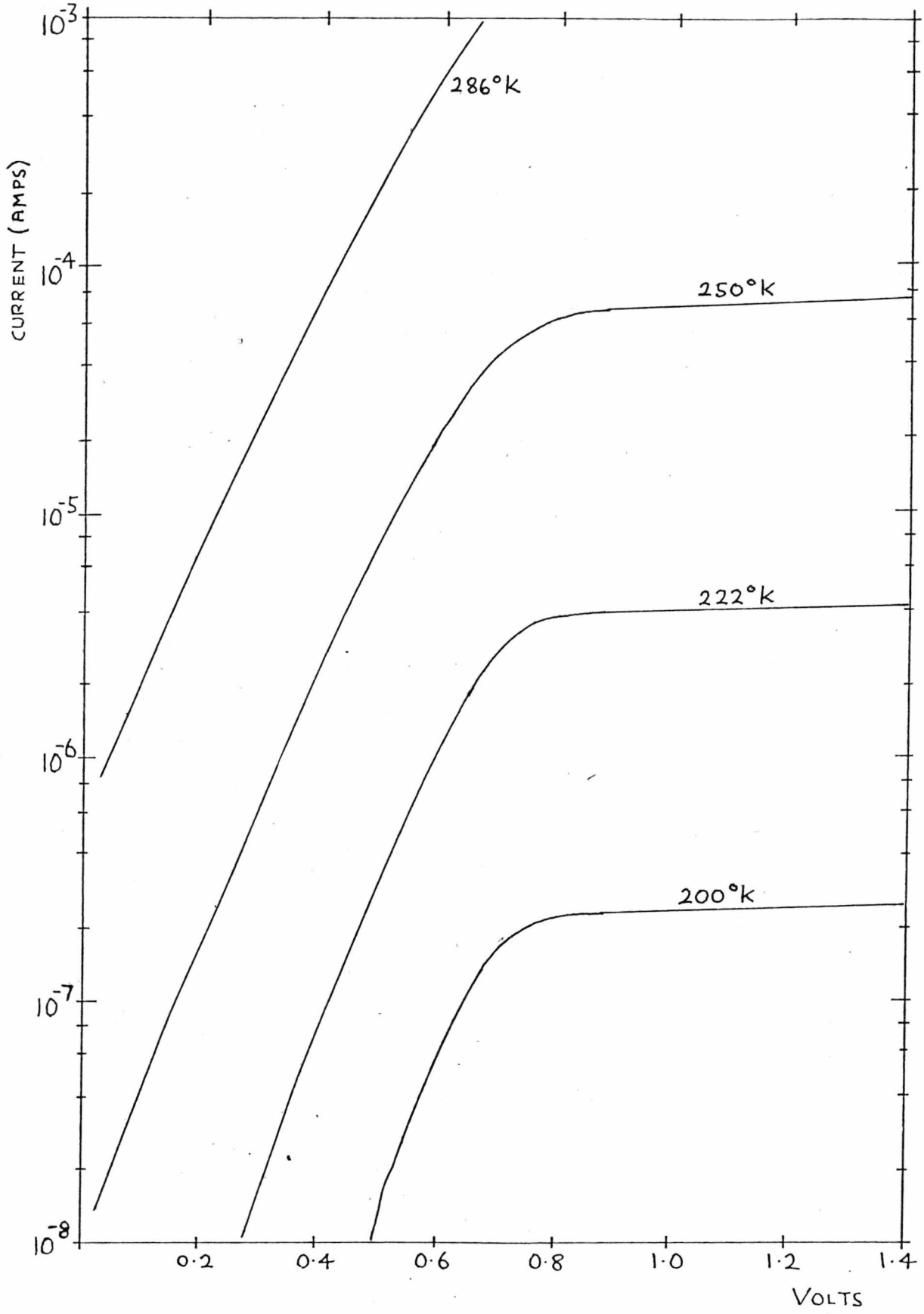


FIGURE 5.20 : Ag-SILICON (HEAT CLEANED) REVERSE BIAS I-V PLOT.

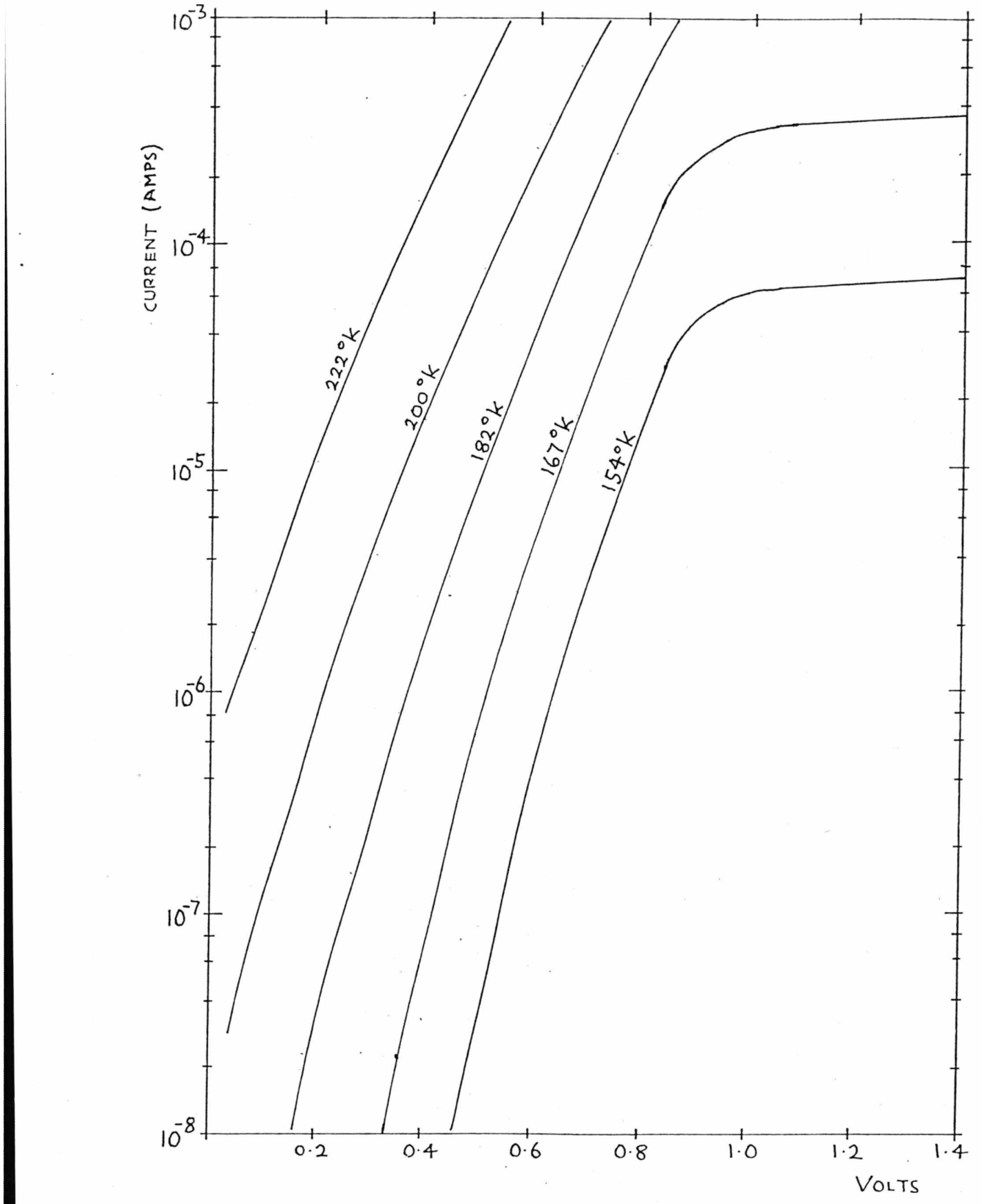


FIGURE 5.21 : Al- SILICON (HEAT CLEANED) REVERSE BIAS I-V PLOT.

CHAPTER 6

INTERPRETATION OF RESULTS

6.1. INTRODUCTION

The usual method of interpreting current flow in metal -semiconductor contacts is to fit the data to the form.

$$I = I_{FB}\left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \qquad (6.1)$$

where n is a dimensionless parameter known as the ideality factor. I_{FB} is the current that would flow under sufficient forward bias to give zero electric field, that is flat band conditions, in the semiconductor. It can be shown[85] that,

$$I_{FB} = aA^{*}T^{2}\exp - (e\phi_b/kT) \qquad (6.2)$$

which is a thermionic component of current with an effective Richardson constant A^{*}[86], a barrier height ϕ_b and device area a.

It is clear that experimental data can be interpreted according to equation (6.1) by plotting ln I against V under forward bias conditions since this should yield a straight line of slope (e/nkT) so that the value of n can be determined. Furthermore the intercept at V = 0 provides a measure of I_{FB} which can be interpreted according to equation (6.2) in order to yield the value of the barrier height ϕ_b. Most measurements reported in the literature are interpreted on this basis.

The basic problem of relying on this method of interpretation is that it relies on a number of assumptions which are:

(i) the thermionic component of current is dominant.

(ii) barrier height dependence on differing bias conditions is successfully accounted for by the ideality factor n being different from unity.

(iii) the barrier height is independent of temperature, T.

These assumptions require some discussion in order to understand the reasons for the particular approach to the data analysis used in this work.

It is well known [87], that current flow between a metal and semiconductor will have a more complex mechanism than just considering thermionic emission alone. This ignores the possibility of quantum mechanical effects at the potential barrier which could result in some electrons at energies below the maximum potential being able to tunnel through and those having energies greater than the barrier maximum suffering partial or quantum mechanical reflections. Such effects can be calculated as a function of the carrier energy and effective mass, the barrier height, electric field at the metal-semiconductor interface, and the shape of the potential barrier at the metal-semiconductor interface[89].

However, these quantum-mechanical effects are usually left as a further deterioration of the ideality factor. It will be seen, in chapter 7, that this leads to problems in understanding the real significance of the barrier height parameter.

It is possible to formulate the form of the bias dependance on barrier height by the well known Schottky theory of image force lowering. The classical derivation implies that $\Delta\phi \propto E_S^{\frac{1}{2}}$, $\Delta\phi$ being the reduction of the barrier height and E_S being the field at the semiconductor interface. Evidence is presented in the literature which supports this approach but it depends however in detail on the exact nature of the contact being considered. In contrast to this approach, Andrews and Lepsetter[88] have produced evidence from a study of silicide forming metal which indicated a barrier height lowering of the form $\Delta\phi \propto E_S$ thereby implying a different expectation for the value of the ideality factor. Thus it must be considered that the concept of the ideality factor may be used to account for a variety of effects which cannot be separated from each other.

It is also worth pointing out that other processes such as generation recombination in the depletion region may under certain conditions have an overriding effect on the current flow. This may be especially dominant at low temperatures and also for the case of small bias conditions. This of course is yet another component to be added to the ideality factor. For these reasons it is not felt appropriate that the method of interpretation based on n can be justified or considered reliable, as current flow characteristic with similar departures from ideality may be due to differing effects, which of course a statement purely based on the value of n cannot distinguish.

It is now worth considering the possibility of barrier height being dependent on temperature. Such a possibility is not usually considered even though it is well known that the energy bands in the semiconductor are temperature dependent as is the value of the metal work function. It might be claimed that equation (6.2) is capable of determining the linear coefficient of the variation of ϕ_b with temperature since this will yield a value of A* which differs from the value expected if ϕ_b is constant with temperature. Even so it is obvious if the possibility of effects due to surface states are to be considered then such a simple temperature dependence may not be considered to be adequate. For example, the field near the semiconductor and hence the barrier height lowering, is through Gauss's theorem, strongly dependent on the charge in the surface states. This charge is in turn governed by the occupational probability which is of course dependent on the Fermi energy of the system. The Fermi energy in the semiconductor is of course temperature dependent with the Fermi level tending to the middle of the band gap at high temperatures. It is clear therefore, that the dependence of ϕ_b on temperature may have important implications on the way in which the current flow information can be interpreted.

6.2. DATA INTERPRETATION CONSIDERATIONS

It is clear from the foregoing discussion that one must approach the question of data interpretation with some caution and just considering an ideality factor will not lead to well defined conclusions being drawn from the current voltage data. It is essential however that we do not go into a formulation considering too many unknowns in the data interpretation as this could lead to more confusion rather than clarity.

It is immediately apparent from the initial probe measurements and from the current-voltage plots, presented in chapter 5, that the characteristics are in considerable disagreement with the thermonic emission theory. However, consideration must be given to the most applicable approach to the data interpretation of the available results.

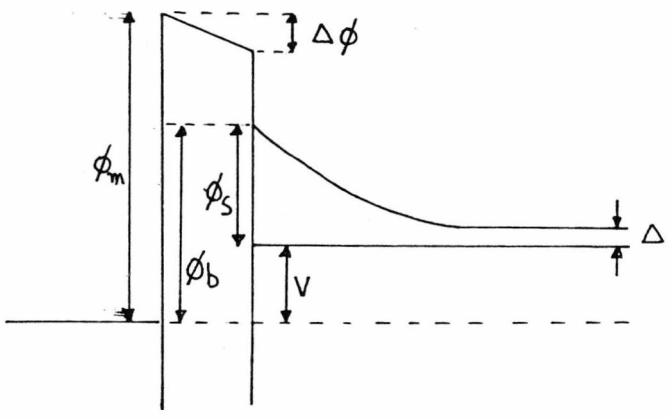
The effects of recombination and generation of electrons and holes in the depletion region were mentioned in the previous section. It is however known (87) (34) that if current transport due to this mechanism is in any way significant this will become apparent in the temperature dependence of the current-voltage characteristics. This recombination/generation current becoming dominant at low temperatures. Thus such a mechanism would be seen to produce increasing non ideal characteristics with

reduction in temperature. From the current voltage plots in chapter 5 this effect is not apparent. It can therefore be stated with some confidence that this is not a dominant mechanism for the devices being considered.

Consideration can now be given to the effects of image force lowering This is usually approximated by an image force lowering term in the thermionic equation such that

$$J_{FB} = A^* T^2 \exp\left[-\frac{e}{kT}(\phi_b - \Delta\phi)\right] \qquad (6.3)$$

where $\Delta\phi$ is the effective reduction in barrier height. When considering this barrier lowering term to be proportional to $E_S^{\frac{1}{2}}$ the effect on the current transport across the interface will only be minimal [87], certainly far less than observed for the devices under consideration. However, the possible effects of this barrier lowering being proportional to E_S [88] should be given some attention. Basic calculations can be performed in order to obtain an estimate as to the order of this effect on the current-voltage characteristics. It should be noted that the following equations are only being considered with this purpose in mind. Consider the band diagram illustrated below



The image force loweing $\Delta\phi$ can be given by

$$\Delta\phi = E_S \, xi$$

where xi is the interfacial thickness.

In this case the barrier height can be given by

$$\phi_b = \phi_m - \chi_S - E_S x_i$$

The variation of barrier height with bias will lead to some indication as to the departures from ideality this model will cause.

$$\frac{\partial \phi_b}{\partial V} = - x_i \frac{\partial E_S}{\partial V} \qquad (6.4)$$

The effects of surface states are not going to be considered at this point. So that E_S can be given by

$$\therefore \frac{\partial E_S}{\partial V} = \frac{eN_o}{\epsilon_i} \frac{\partial W}{\partial V} \qquad (6.5)$$

$$\phi_S = \frac{eN_oW^2}{2\epsilon_S} = (\phi_m - E_S x_i - \Delta - V - \chi_S)$$

$$= \phi_m - \frac{e N_o W x_i}{\epsilon_i} - \Delta - V - \chi_S$$

$$\therefore \frac{eN_oW^2}{2\epsilon_s} + e\frac{N_oW}{\epsilon_i} x_i - \phi_m - \chi_S - V - \Delta = 0$$

It can be considered that $W \gg x_i$ therefore

$$W \simeq \sqrt{2\epsilon_S \frac{(\phi_{bo} - V - \Delta)}{eN_o}}$$

$$\therefore \frac{\partial W}{\partial V} \simeq - \frac{1}{2W} \left(\frac{2\epsilon_s}{eN_o}\right)$$

using this result in equation (6.5) and then (6.4)

$$\frac{\partial \phi_b}{\partial V} \simeq - \frac{eN_o x_i}{\epsilon_i} \frac{\epsilon_S}{WeN_o}$$

for an estimate consider $\frac{x_i}{W} \sim 10^{-2}$ and $\frac{\epsilon_S}{\epsilon_i} \sim 3$

$$\therefore \frac{\partial \phi_b}{\partial V} \simeq -3 \times 10^{-2}$$

The order of ideality factor to be expected from this variation can be determined by considering the normal method of fitting data to equations (6.1) and (6.2)

$$\log I = \log (A^*T^2) + \frac{e\phi_b}{kT} + \frac{eV}{kT}$$

$$\frac{\partial \log I}{\partial V} = \frac{e}{kT}\left(\frac{\partial \phi_b}{\partial V} + 1\right)$$

$$\therefore \frac{1}{n} = \left(\frac{\partial \phi b}{\partial V} + 1\right)$$

Thus it can be seen that this will result in only a small departure from ideality.

However, it is well known (90) that when considering a contact involving surface states, due to whatever cause, there will be considerable variations in barrier energy with bias. The charge at the surface is dependent upon the relative position of the Fermi level and the neutral level of the surface states. With the variation of surface charge with applied bias, significant variation in the barrier profile at the interface can be expected. This effect can perhaps be best observed by a study of the reverse characteristics of the contacts involving low metal work functions. The very soft reverse bias characteristics typical of significant lowering of the barrier energy thus leading to far higher reverse current than would normally be considered. This effect can easily be seen in the I - V plots in chapter 5. It could however be stated that breakdown conditions are being observed. However, consideration of the equations below indicate this not to be the case.

For silicon the breakdown voltage is given by

$$V_b = 60 \left(\frac{N_I}{10^{22}}\right)^{-\frac{3}{4}}$$

the maximum electric field

$$E_m = \frac{2V}{W} = \frac{2V}{\sqrt{2\epsilon_S V/eN_I}} = \sqrt{\frac{2\,eN_I V}{\epsilon_S}}$$

Thus the breakdown field will be given by

$$E_b = \sqrt{\frac{2eN_I}{\epsilon_S}} \left(60 \left[\frac{N_I}{10^{22}}\right]^{-\frac{3}{4}}\right)$$

This can be approximated to the expression below

$$E_b \simeq 7.8\ N_I^{1/8} \times 10^4\ V/m$$

Consideration can be given to the two forms of interface examined during this work.

For the epitaxial layer contacts.

$$N_I \simeq 1.6 \times 10^{22}\ cm^{-3}$$

From the equations above, using this doping density a breakdown field of the order of $4.5 \times 10^7 V/m$ at a depletion layer width of less than $2\mu m$ can be expected. These values are well within the epitaxial layer thickness and voltages considered during this work.

For the heat cleaned surface contacts.

$$N_I \simeq 3 \times 10^{20}\ cm^{-3}$$

For this case the breakdown field is of the order of 3×10^7 V/m at a depletion layer width of $59\mu m$.

Also for breakdown conditions the characteristics would be hard which is not the observed case. It is also interesting to note that the normal reverse bias saturation conditions are not present thus further suggesting a lowering of the barrier height with reverse bias. It is therefore felt confident that the data can be interpreted in terms of the variation of the barrier height with bias.

6.3. DETAILS OF DATA INTERPRETATION

From the considerations discussed in this chapter, the experimental values for barrier height and the variation of barrier height with applied voltage can be determined for the metal-silicon contacts under investigation. A graphical solution can be determined by the use of the usual log I versus voltage plots as indicated in figure 6-1. Values of $\Delta\phi$, the variation of barrier height with applied voltage, can be directly obtained from such a plot. The slope of the graph will yield a value of $e\ (1 - \Delta\phi)/kT$ so that $\Delta\phi$ can be determined for each metal-silicon contact over the temperature range investigated. The flat band current I_{FB} can be determined from this plot by extrapolation to $V = 0$ where I_{FB} is given by equation (6.2). If this value is measured as a function of temperature and $\log (I_{FB}/T^2)$ plotted as a function of $1/T$, this Richardson plot will give values of A^* and ϕ_b. However this can only be considered valid if the zero bias barrier height is independent of temperature. Therefore in the absence of an explicit

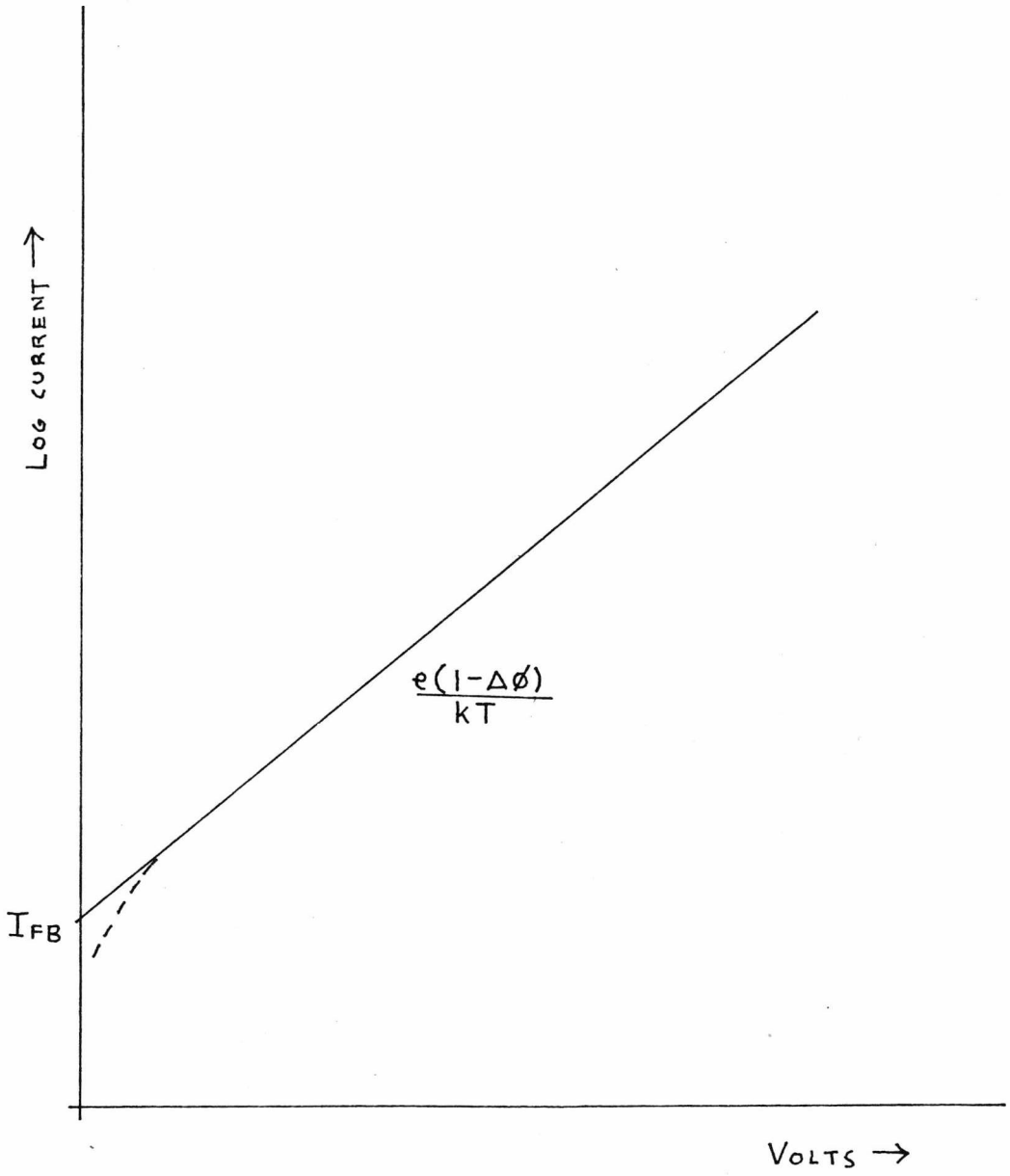


FIGURE 6.1 : GRAPHICAL DETERMINATION OF $\Delta\phi$ AND I_{FB}

measurement of ϕ_b as a function of temperature, the Richardson plot yields[125].

$$A^* \exp\left(-\frac{e}{k}\frac{d\phi_b}{dT}\right) \text{ and } \phi_b(T) - T\left(\frac{d\phi_b}{dT}\right)$$

The situation becomes further complicated if the temperature dependence is not linear. Therefore without an accurate independent measurement of ϕ_b the above approach cannot be expected to provide a check on the theoretical value of A^*. In this situation the best approach is to assume a value of A^* in order to determine the temperature dependence of ϕ_b directly from the values obtained for I_{FB}. The value used for A^* was 259 $Amp/cm^2/^oK^2$. This value being reported by Crowell[86] who determined A^* for a variety of semiconductor tensor effective masses. The value of the Boltzmann constant k being 8.614×10^{-5} eV/K.

In practice a simple curve fitting programme was used in order to obtain the best fit to the experimental points on the log I versus voltage plot. The following set of tables, figures 6.2 to 6.9 list all the results determined from the current voltage data presented in chapter 5. Several contacts of each type were characterised and the errors quoted for the results obtained give the standard deviations of the mean values.

TEMP (°k)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
364 ± 0·5	0·817 ± 0·005	0·279 ± 0·01
333 ± 0·5	0·823 ± 0·005	0·281 ± 0·01
308 ± 0·5	0·826 ± 0·005	0·284 ± 0·01
286 ± 0·5	0·828 ± 0·005	0·284 ± 0·01
267 ± 0·5	0·830 ± 0·005	0·284 ± 0·01
250 ± 0·5	0·829 ± 0·005	0·285 ± 0·01

FIGURE 6.2 : AU-EPITAXIAL LAYER RESULTS.

TEMP (°K)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
333 ± 0·5	0·675 ± 0·005	0·303 ± 0·01
286 ± 0·5	0·682 ± 0·005	0·306 ± 0·01
250 ± 0·5	0·684 ± 0·005	0·312 ± 0·01
222 ± 0·5	0·687 ± 0·005	0·316 ± 0·01
200 ± 0·5	0·688 ± 0·005	0·318 ± 0·01
182 ± 0·5	0·689 ± 0·005	0·320 ± 0·01

FIGURE 6.3 Cr-EPITAXIAL LAYER RESULTS.

Temp (°K)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
286 ± 0·5	0·635 ± 0·005	0·302 ± 0·01
250 ± 0·5	0·640 ± 0·005	0·302 ± 0·01
222 ± 0·5	0·645 ± 0·005	0·306 ± 0·01
200 ± 0·5	0·647 ± 0·005	0·310 ± 0·01
182 ± 0·5	0·648 ± 0·005	0·310 ± 0·01
167 ± 0·5	0·648 ± 0·005	0·312 ± 0·01

Figure 6.4 : Ag - epitaxial layer results.

Temp (°K)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
250 ± 0·5	0·491 ± 0·005	0·322 ± 0·01
222 ± 0·5	0·493 ± 0·005	0·327 ± 0·01
200 ± 0·5	0·496 ± 0·005	0·331 ± 0·01
182 ± 0·5	0·498 ± 0·005	0·333 ± 0·01
167 ± 0·5	0·498 ± 0·005	0·336 ± 0·01
154 ± 0·5	0·499 ± 0·005	0·343 ± 0·01

Figure 6.5 : Al - epitaxial layer results.

Temp (°k)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
364 ± 0·5	0·823 ± 0·005	0·281 ± 0·01
333 ± 0·5	0·827 ± 0·005	0·284 ± 0·01
308 ± 0·5	0·830 ± 0·005	0·284 ± 0·01
286 ± 0·5	0·832 ± 0·005	0·285 ± 0·01
267 ± 0·5	0·834 ± 0·005	0·285 ± 0·01
250 ± 0·5	0·836 ± 0·005	0·287 ± 0·01

Figure 6.6 : Au-silicon (heat cleaned) results.

Temp (°k)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
333 ± 0·5	0·685 ± 0·005	0·301 ± 0·01
286 ± 0·5	0·688 ± 0·005	0·308 ± 0·01
250 ± 0·5	0·691 ± 0·005	0·316 ± 0·01
222 ± 0·5	0·693 ± 0·005	0·324 ± 0·01
200 ± 0·5	0·695 ± 0·005	0·332 ± 0·01
182 ± 0·5	0·696 ± 0·005	0·335 ± 0·01

Figure 6.7 : Cr-silicon (heat cleaned) results.

Temp (°k)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
286 ± 0·5	0·644 ± 0·005	0·305 ± 0·01
250 ± 0·5	0·648 ± 0·005	0·308 ± 0·01
222 ± 0·5	0·650 ± 0·005	0·312 ± 0·01
200 ± 0·5	0·652 ± 0·005	0·315 ± 0·01
182 ± 0·5	0·654 ± 0·005	0·320 ± 0·01
167 ± 0·5	0·655 ± 0·005	0·322 ± 0·01

Figure 6.8 : Ag-silicon (heat cleaned) results.

Temp (°k)	ϕ_b (eV)	$\Delta\phi$ (eV/V)
250 ± 0·5	0·497 ± 0·005	0·328 ± 0·01
222 ± 0·5	0·500 ± 0·005	0·335 ± 0·01
200 ± 0·5	0·502 ± 0·005	0·337 ± 0·01
182 ± 0·5	0·504 ± 0·005	0·339 ± 0·01
167 ± 0·5	0·506 ± 0·005	0·344 ± 0·01
154 ± 0·5	0·507 ± 0·005	0·348 ± 0·01

Figure 6.9 : Al-silicon (heat cleaned) results.

CHAPTER 7

THEORETICAL ANALYSIS

7.1. SILICON SURFACE STRUCTURE

As the cleanliness of the surface of the silicon substrates is of prime importance in this work, it is therefore necessary to consider the atomic structure of such a surface. It is obviously not possible to carry out an in depth study of the surface structure of silicon in this thesis, but it is of interest to outline the various theoretical models that have been put forward. This of importance in order to obtain some correlation with the experimental observations of clean silicon surfaces, thereby obtaining a certain degree of confidence as to the atomic cleanliness of the surfaces prepared during this work.

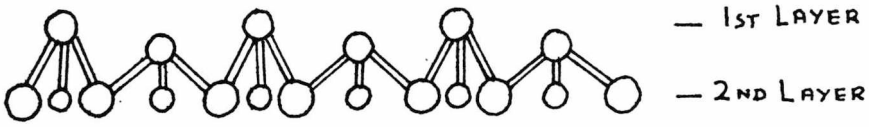
When considering the surface structure of silicon one must take into account what positions the atoms occupy in the surface, and how they are bound to neighbouring atoms. Also of importance is whether the stable surface structure is intrinsic or impurity stabilised. It would appear from low energy diffraction measurements that a clean silicon surface has atom arrangements different from that of corresponding bulk planes. It is however difficult to definitely establish the surface structure. A number of experiments have been reported which provide indirect evidence. These involve measurements of LEED[37,38,94,95,96,97,98], surface state properties[64], spin resonance[99] and surface mating characteristics[100], LEED clearly shows a super-structure to exist on both cleaved and thermally cleaned surfaces, but the superstructures are different. The cleaved surface gives a silicon (2 x 1) pattern, which can be converted to a silicon (7 x 7) pattern by a high temperature anneal in what is apparently an activated process, possibly surface diffusion of vacancies. Annealing at low temperatures produces a silicon (1 x 1) pattern. Thermal cleaning produces first silicon (1 x 1) and then silicon (7 x 7) as the temperature is increased. It is however difficult to establish whether these patterns are intrinsic or impurity stabilised.

Two basic theoretical models have been proposed for an intrinsic silicon surface structure. Both involve a surface which is modified with respect to simple termination of the bulk lattice. Lander and Morrison[37] proposed a surface model which basically describes the surface in terms of warped conjugated rings with one quarter of the top layer of atoms missing. Seiwatz[101] proposed a modification to this model with the surface having conjugated chains rather than rings.

Most recent discussions however seem to favour a model based on the periodic raising and lowering of rows of surface atoms leaving a buckled surface. This model was first suggested by Haneman[96] and later developed by Taloni and Haneman[102]. In addition to the periodic raising and lowering of surface atoms, in Haneman's model, the second layer atoms are slightly shifted laterally in order to approximately conserve the individual bond lengths of the traverse back bonds between the first and second layer. Haneman's basic model is illustrated in figure 7.1. As can be seen from the diagram the surface unit cell is (2 x 2), but the (7 x 7) surface unit cell, which is the structure of annealed clean silicon surfaces, could be made up by appropriate combinations of the (2 x 2) unit cell[103] predicted by the Haneman model.

Although it is not possible to distinguish between the various alternatives by a strict interpretation of LEED intensity data, the Haneman model seems more likely on purely chemical grounds[65]. Firstly Si = Si bonds are not found in any silicon compounds, and secondly many adsorption experiments show that the adsorbate assumes a monolayer structure corresponding to the normal number of silicon atoms in the surface.

It has been suggested that the (7 x 7) pattern could arise from an epitaxial surface layer of hexagonal $Fe_5 Si_3$ on the silicon[104]. The origin of the iron was considered to be out diffusion from the bulk. However, it has been shown[105,106] that the (7 x 7) pattern can be formed so quickly after cleavage at comparitively low temperatures, that from the known solid solubility and diffusivity data for iron in silicon the required amount of iron could not accumulate at the surface. Work has been carried out[107] to try and correlate the (7 x 7) superstructure with heavy metal impurities. From the work of Monch[108] it would however appear that the (7 x 7) superstructure is not associated with heavy metal impurities. He determined that the conversion temperature from the unstable (2 x 1) to the stable (7 x 7) structure could be as low as 370°C and no heavy metal impurities could be observed by the use of Auger.



SECTIONAL VIEW OF (111) SURFACE ACCORDING TO H MODEL.

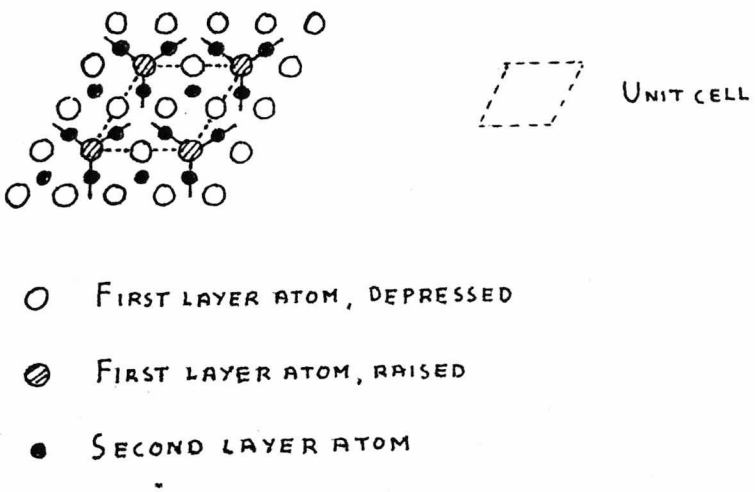


FIGURE 7.1 : TOP VIEW OF H MODEL SURFACE.

To conclude it would seem reasonable from the theoretical and experimental observations that the silicon (7 x 7) structure is an intrinsic stable silicon surface structure. This is of course important as the thermally cleaned surfaces used in this research work exhibit this surface structure. Thus it can be said with some confidence that the metal contacts are being formed onto a clean near ideal silicon surface.

7.2. SURFACE STATES

The existence of states, within the silicon forbidden band-gap, localised at the surface has long been recognised. Much experimental and theoretical analysis has been carried out on the effects of these surface states, showing that they play an important role in the determination of the nature of the potential barrier in metal-silicon rectifying systems.

Surface states on clean silicon surfaces can be related to a number of different causes. Tamm[2] initially realised that the termination of the periodic potential at the surface must give rise to certain modifications of the band structure. By a very basic theoretical analysis he showed that this termination at the surface would lead to the existence of allowed levels within the semiconductor band-gap. Shockley[3] and Statz[109] carried out a more detailed theoretical analysis on these lines. According to the model proposed by Shockley one discrete surface state should arise for each surface atom if the lattice spacing is sufficiently small. There may also exist dangling bonds[110] if they are not saturated by foreign atoms or by a change in the crystal structure in the uppermost layers of atoms[111]. Also the changed structure at the surface, as discussed in the previous section, can give rise to electronic states with energies in the forbidden gap of the semiconductor. A similar effect is attributed to a damaged lattice which may remain from an ion bombardment or cleavage cleaning procedure.

Bardeen[4] considered the effects of these surface states on the rectification characteristics of a metal-semiconductor contact. He showed that if the density of these localised states is sufficiently high, a double layer at the free surface of the semiconductor is formed from a net charge of electrons in surface states and a space charge of opposite sign. He concluded that this double layer will tend to make the work function independent of the Fermi level in the interior of the semiconductor. Thus the rectification characteristics of a metal-semiconductor contact are then practically independent of the metal used.

This can be simply outlined by considering the band diagram of a metal semiconductor contact as shown in figure 7.2. For this purpose we will consider that the surface states are continuously distributed in energy within the forbidden gap. These states are characterised by a 'neutral level' ϕ_o such that if the surface states are occupied up to ϕ_o and empty above ϕ_o the surface is electrically neutral. If we approximate the Fermi Dirac distribution by a step function, it follows then when the Fermi level E_F lies above ϕ_o the surface states possess a net negative charge, while if E_F lies below ϕ_o they possess a net positive charge. In other words, the states below ϕ_o are donor like, positive when empty, and the states above ϕ_o are acceptor like, negative when occupied. For the case shown in figure 7.2, in which $\phi_o > E_F$, there is a net positive charge in the surface states. This means that some of the lines of force terminating on the metal eminate from the surface charges rather than the ionized donors, in this case the space charge region is not as thick as when the surface states are absent, and consequently the barrier height will be reduced. In the same way, if $\phi_o < E_F$ then there will be a net negative charge in the surface states and the barrier height is increased. Thus the charge in the surface states has a kind of negative feedback effect which always tends to reduce the deviation of ϕ_o from E_F. If the density of surface states is very high, the gain in the feedback loop will be very large, and ϕ_o will tend to be locked to E_F so that the barrier height will be virtually independent of the metal used.

7.3. BASIC SURFACE STATE ANALYSIS

The following basic mathematical analysis outlines the effects of surface states on the determination of the barrier height in a metal semiconductor contact. Also considered is how this effect is dependent on the density of the surface states. Again referring to the band diagram of a metal-semiconductor contact as illustrated in figure 7.2, where the metal and semiconductor are separated by a thin interfacial layer of thickness δ. Assuming a uniform distribution of surface states within the energy gap with a density D_S cm^{-2} eV^{-1}, the surface state charge Q_{SS} cm^{-2} can then be given by

$$Q_{SS} = -eD_S (E_G - \Delta - \phi_o - eV_D) \qquad (7.1)$$

where ϕ_o denotes the position of the neutral level of the surface states with respect to the top of the valence band.

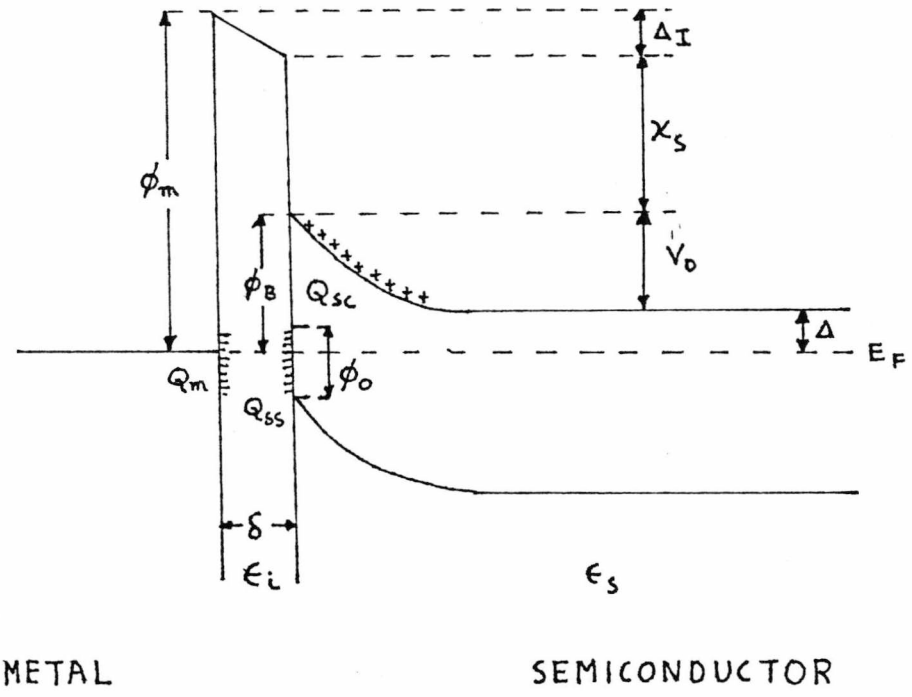


FIGURE 7.2 : ENERGY BAND DIAGRAM.

The distributed charge in the depletion region, Q_{SC}, can be determined by solving Poisson's equation within the barrier.

i.e. $$Q_{SC} = \epsilon_S E_S \tag{7.2}$$

where E_S is the field in the depletion region and is given by:

$$E_S = \frac{eN_D W}{\epsilon_S} \tag{7.3}$$

W is the depletion width and this is given by:

$$W = \left[\frac{2\epsilon_S (V_D - V)}{eN_D} \right]^{\frac{1}{2}} \tag{7.4}$$

where V is the applied voltage

where N_D is the donar density in the semiconductor thus from equations (7.3) and (7.4)

$$E_S = \left[\frac{2eN_D (V_D - V)}{\epsilon_S} \right] \tag{7.5}$$

$\therefore$ at $V = 0$

$$E_S = \left[\frac{2eN_D V_D}{\epsilon_S} \right] \tag{7.6}$$

$$\therefore Q_{SC} = \epsilon_S E_S = (2\epsilon_S eN_D V_D)^{\frac{1}{2}} \tag{7.7}$$

The total equivalent surface charge density on the semiconductor surface is given by the sum of equations (7.1) and (7.7). In the absence of any space charge effects in the interfacial layer, on exactly equal and opposite charge Q_m develops on the metal surface. For thin interfacial layers, such effects are negligible, and Q_m can be written as;

$$Q_m = -(Q_{SS} + Q_{SC}) \tag{7.8}$$

The charge on the metal surface, Q_m, can be determined by applying Gauss's law to the intervening layer between the metal and semiconductor.

$$Q_m = \frac{-\Delta_I \epsilon_i}{\delta} \tag{7.9}$$

where Δ_I is the potential across the interfacial layer.

Δ_I can be obtained by the inspection of the energy band diagram in figure 7.2.

i.e. $$\Delta_I = \phi_m - \chi_s - \Delta - eV_D \tag{7.10}$$

Therefore from equations (7.9 and (7.10) we can obtain an expression for Q_m.

$$Q_m = \frac{-\epsilon_i}{\delta} (Q_m - \chi_S - \Delta - eV_D) \tag{7.11}$$

Thus if $-Q_m$ and $Q_{SS} + Q_{SC}$ are plotted together on the same graph as a function of V_D (figure 7.3) then the intercept gives the value of V_D for the particular value of δ, ϵ_i, ϵ_S, D_S and ϕ_m. From this graph it can be seen that if D_S is very large then the slope of $Q_{SS} + Q_{SC}$ becomes very great and thus the barrier height of the metal semiconductor contact becomes almost exclusively dependent on the position of the neutral level ϕ_o in the semiconductor band gap. At the other extreme, with a low D_S, the barrier height will then obey the classical Schottky equation.

$$\phi_b = \phi_m - \chi_S \tag{7.12}$$

From the above considerations Cowley and Sze [5] obtained the following expression for the barrier height.

$$\phi_b = \gamma(\phi_m - \chi_S) + (1 - \gamma)(E_g - \phi_o) \tag{7.13}$$

where γ is dependent on the surface state density and the interfacial layer thickness.

For an extremely low value of D_S $\gamma \rightarrow 1$

For a very high value of D_S $\gamma \rightarrow 0$

Thus as before it can be seen that for $\gamma = 1$ we have the same relationship as equation (7.12)

For $\gamma = 0$ we obtain

$$\phi_b = E_g - \phi_o \tag{7.14}$$

In this case the Fermi level at the interface is pinned by the surface states at the value ϕ_o above the valence band.

From this basic analysis it can be seen that the surface state density and the neutral level of these states play a very dominant role in the determination of the barrier height. Considering that metal-silicon contacts do not obey the Schottky relationship in equation (7.12) it is therefore of great importance in the interpretation of the characteristics of the contacts produced in this work to seriously analyse the effects of these surface states on the nature of the potential barrier in the metal-silicon contacts formed.

7.4. INTIMATE METAL-SILICON CONTACTS

It can be seen from the preceeding analysis of the effects of surface states on the barrier heights of metal semiconductor contacts that the existence of an interfacial layer is essential to this theoretical model. This analysis is of course valid for interfaces formed by the deposition of a metal film onto a chemically cleaned semiconductor surface as there will always be a thin interfacial oxide layer present with this technique. However, with regards to the present work undertaken, the interfaces were formed by U.H.V. heat

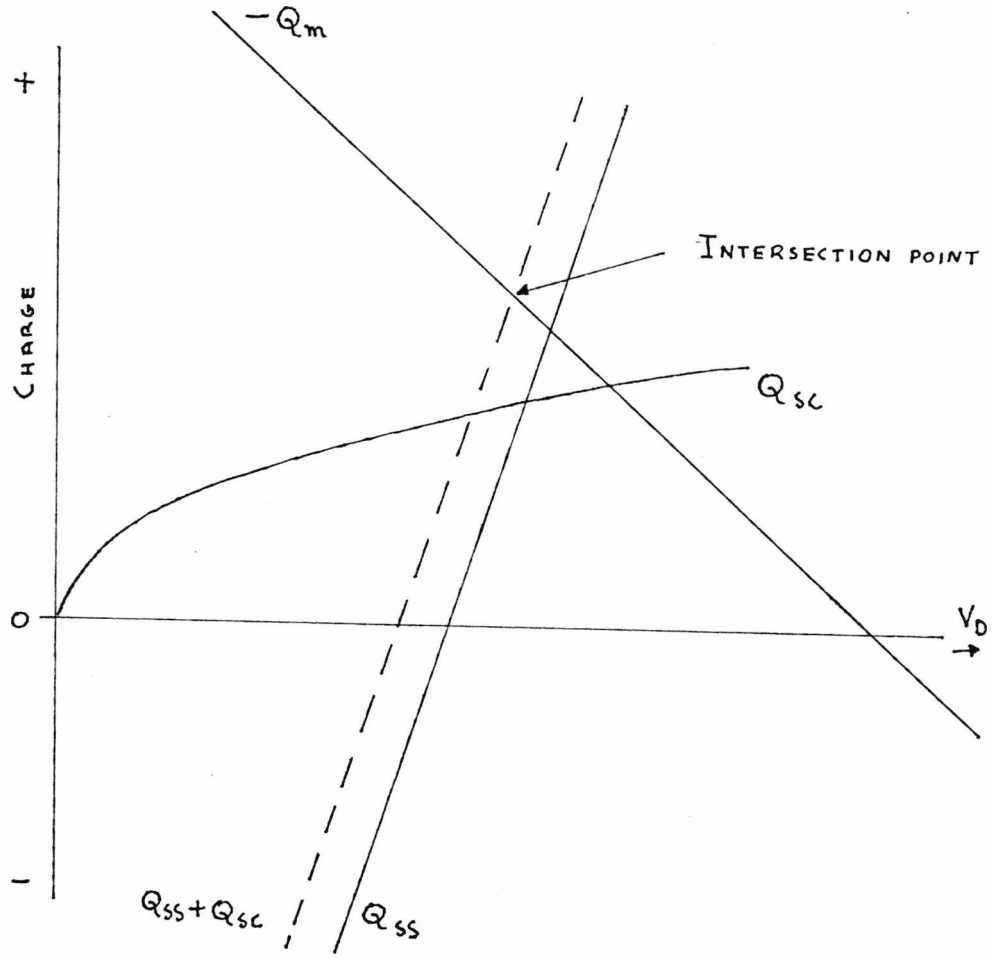


FIGURE 7.3 : Q - V_D RELATIONSHIPS AT METAL-SEMICONDUCTOR INTERFACE.

cleaning and the metal contact also formed under U.H.V. conditions. Thus we are considering an intimate metal-silicon contact and this basic surface state model cannot really be applied to the interfaces formed during this present work. Heine[6,112,113,114] pointed out that these surface states, as considered in the previous section, have no meaning for the case of an intimate metal-semiconductor contact. Heine's original work was to consider the effects of the metal quantumstates tailing into the forbidden gap of the semiconductor in intimate metal-semiconductor contacts, thus producing a similar effect as the surface states already discussed. The basic concept of Heine's original theoretical model can be illustrated by considering the E - K diagrams for a metal and a semiconductor as shown in figure 7.4. For an energy E below E_F in the semiconductor band-gap, the solutions of the Schrodinger equation will decay exponentially in the semiconductor but propogate as Bloch states on the metal side of the function to form the ordinary volume states of the metal. This follows from simple considerations of matching the wave functions at the boundary. For some value of $K = K_{||}$ parallel to the surface e.g. $K_y = K_Z = 0$ we have bands as shown in figure 7.4. At energy E, the exponential solution in the semiconductor can always be joined onto the two Bloch states withwave vector $K_{\perp}$, $= K_1, -K_1$ in the metal. The existence of the two K's ensuring that both ψ and its derivative can be matched at the boundary. Thus for energies in the semiconductor band-gap the volume states of the metal all have tails in the semiconductor and there are actually no surface states.

The following theoretical model proposed is based on this original work of Heine's related to the analysis of the intimate metal-silicon interfaces formed during this work.

7.5. THEORETICAL MODEL

In this theoretical analysis we can combine the surface state charge effects with the effects of the space charge in order to determine the potential distribution across the depletion region, thus leading to a determination of the barrier profile

It is possible to describe the surface state charge by a density.

$$\rho_S = en_S(X) \tag{7.15}$$

where $n_S(X)$ represents the effective density of positive charge centres.

It can be assumed that the quantum tails from the metallic wave functions penetrate the semiconductor to a mean depth X_o, where X_o is defined as

$$n_S(X_o)/n_{S(o)} = e^{-1} \tag{7.16}$$

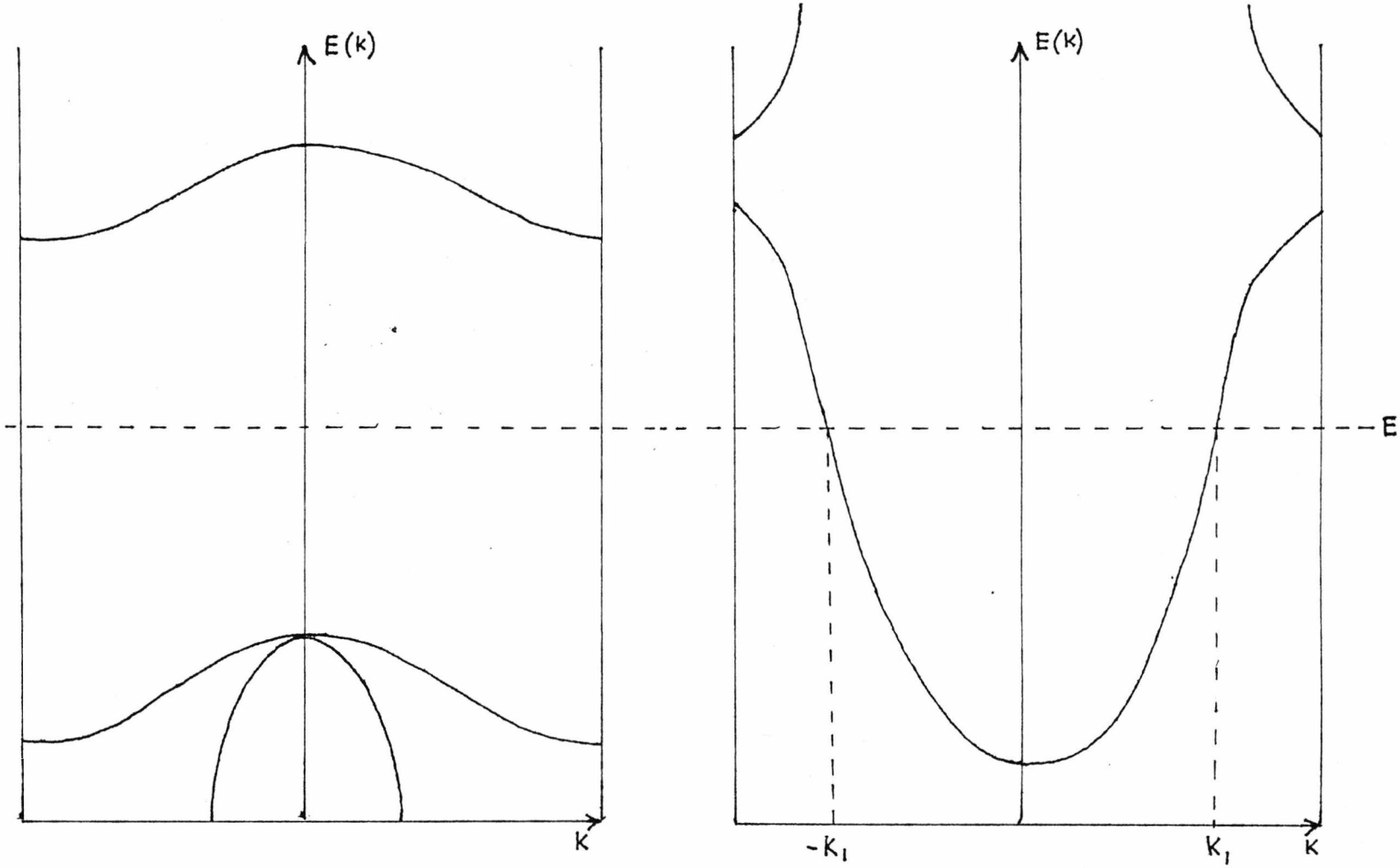


FIGURE 7.4 : E-K DIAGRAMS.

If a surface state density parameter N_{SS} is introduced as the number of charge centres per unit area then.

$$n_S(X) = \frac{N_{SS}}{X_o} \exp - (X/X_o) \qquad (7.17)$$

This charge distribution of the penetrating tails into the semiconductor band-gap is illustrated in figure 7.5. This is essentially the exponential decay expected for the surface charges as proposed by Heine[6] where X_o can be expected to be of the order of 3 to 4 A^o for the case of silicon.

If the metal is in contact with a semiconductor having a donor density N_D then the space charge density can be given by.

$$\rho = e\left\{N_D + \frac{N_{SS}}{X_o} \exp - \left(\frac{X}{X_o}\right)\right\} \qquad (7.18)$$

Integration with respect to X leads to the electric field distribution.

$$E(X) = {}^{e}/_{\epsilon S}\left\{N_D\ (X - W) - N_{SS}\left[\exp\left(-X/X_o\right) - \exp\left(\frac{-W}{X_o}\right)\right]\right\} \qquad (7.19)$$

and a potential distribution

$$\psi(X) = \frac{e}{\epsilon S}\left\{N_D\ \frac{(X-W)^2}{2} + N_{SS}\ X_o\ \left[\exp\left(-X/X_o\right) - \exp\left(-W/X_o\right)\right]\right.$$
$$\left. + N_{SS}\left(X - W\right)\exp\left(\frac{-W}{X_o}\right)\right\} \qquad (7.20)$$

in which the boundary condition is $E(W) = \psi(W) = 0$ where W is the width of the depletion region.

7.5.1. DISTRIBUTION OF SURFACE STATES:-

In the basic surface state analysis[5], a uniform distribution of surface states across the energy band-gap was assumed. However, for both the metal induced surface states and also the intrinsic surface states this is not the case. From experimental analysis[115] and also the theoretical analysis by Heine[6] leading to the later more detailed computation of Louie, Chelikowsky and Cohen[15], the surface states have a distribution of the form shown below.

$$D_{SS} = D_{SO}\ C_{osh}\ C2/e\left(E - E_o\right) m^{-2}\ eV^{-1} \qquad (7.21)$$

this distribution is illustrated in figure 7.6.

This implies a surface state density of the form

$$N_{SS} = \int_{e\phi_s}^{e\phi_o} D_{SS}\, dE + N_{SO} \qquad (7.22)$$

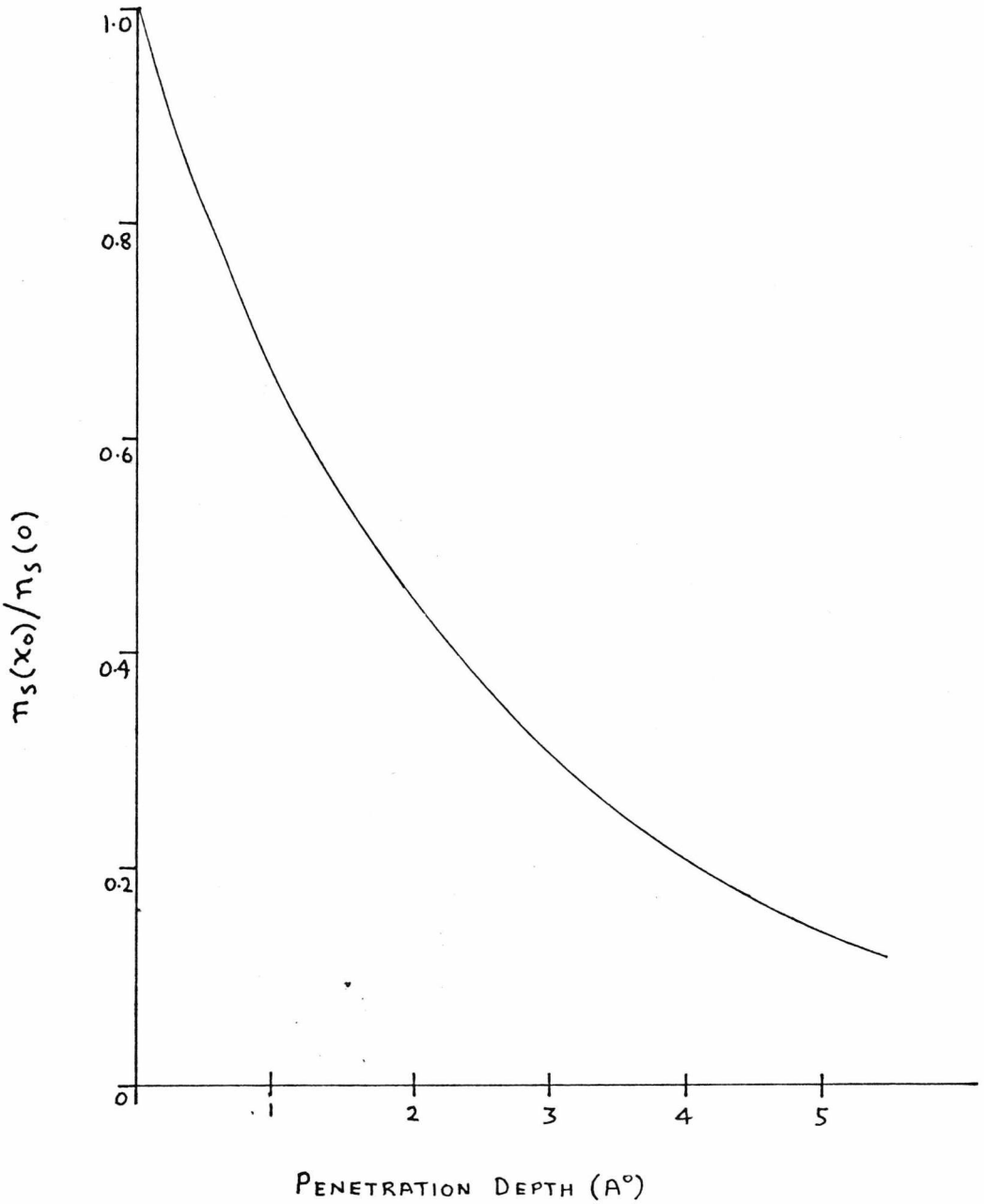


FIGURE 7.5 : CHARGE DISTRIBUTION OF THE PENETRATING METALLIC QUANTUM STATES.

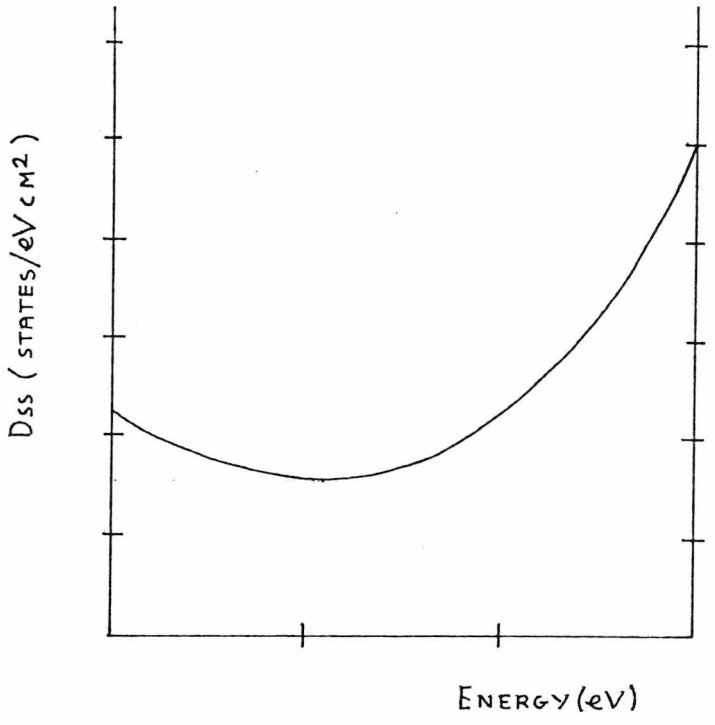


FIGURE 7.6 : VARIATION OF THE DENSITY OF SURFACE STATES IN THE SEMICONDUCTOR BAND-GAP

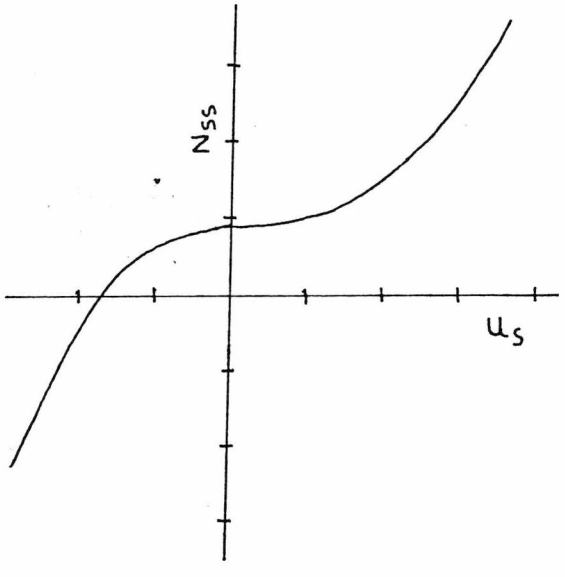


FIGURE 7.7 : VARIATION OF N_{ss} WITH U_s .

where $E_o = e\phi_o$ and N_{SO} is the surface state density attributed to the presence of surface impurities or defects

that is:-

$$N_{SS} = N_S \sinh C_2 (\phi_o - \phi_S) + N_{SO} \qquad (7.23)$$

This is a similar expression to that obtained experimentally by Allen and Gobeli[115] in their work on the surface state density for atomically clean silicon (apart from N_{SO}). ϕ_S and ϕ_o are the position of the Fermi level and the position of the "neutral level" of the surface states respectively in the semiconductor band-gap. Thus we can define U_S as

$$U_S = (\phi_o - \phi_S) \qquad (7.24)$$

$$\text{then} \quad N_{SS} = N_S \sinh (C_2 \; U_S) + N_{SO} \qquad (7.25)$$

This variance of surface state density with respect to U_S is illustrated in figure 7.7.

7.5.2. ENERGY B AND DIAGRAM:-

The depletion layer width W follows from the boundary condition.

$$\psi (0) = -(\phi_{bo} - V - \Delta) \qquad (7.27)$$

in which $\phi_{bo} = \phi_m - \chi_s$ at $\psi (0)$ is defined from equation (7.20) which is the classical Shockley relationship. ϕ_m is the work function of the metal and χ_s is the electron affinity of the semiconductor.

Thus a solution for the depletion layer width can be obtained from

$$W = \left[2\epsilon_S \frac{(\phi_{bo} - V - \Delta)}{eN_D} - \frac{2 N_{SS} X_o}{N_D} \right]^{\frac{1}{2}} \qquad (7.28)$$

The energy band diagram for the case $V > O$ and $N_{SS} < O$ is illustrated in figure 7.8. From this diagram it can be seen that the surface state effect can be assumed to create a form of intermediate region of extent which is small compared to W, so that the location of E_o with respect to the position of the conduction band edge in the bulk semiconductor, is given by.

$$E_o = e\phi_o = \frac{e^2 N_D W^2}{2\epsilon_S} - E_{CS}$$

where E_{CS} is given by the position of E_o with respect to the barrier maximum in the intermediate region.

$$\text{i.e.} \quad \phi_o = \frac{eN_D W^2}{2\epsilon_S} - \frac{E_{CS}}{e}$$

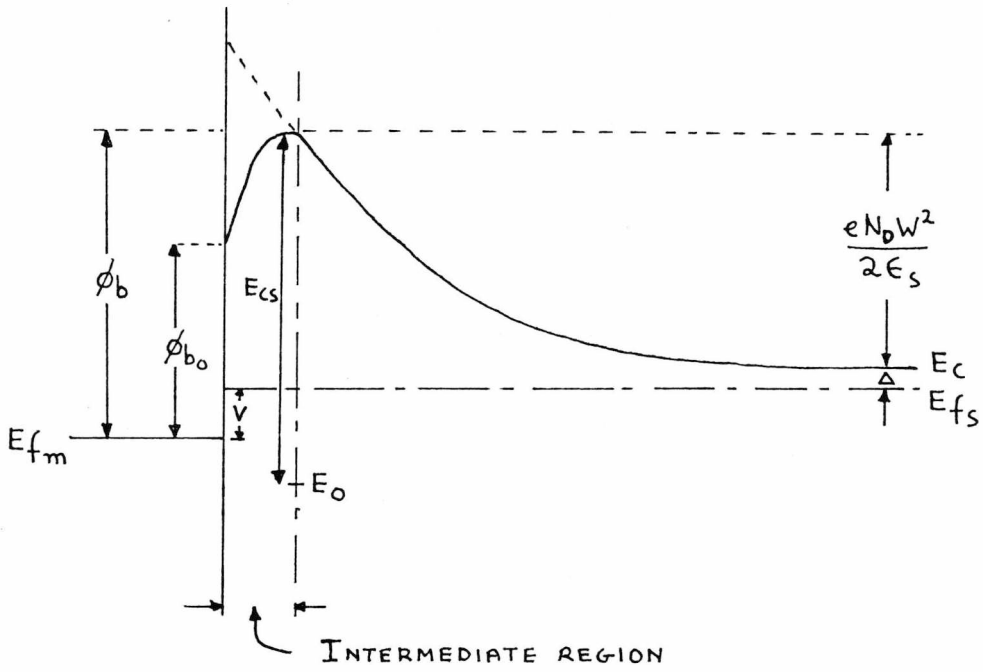


FIGURE 7.8 : BAND DIAGRAM FOR V>0 AND Nss<0 .

From equation (7.28) we have

$$\frac{e N_D W^2}{2\epsilon_S} = (\phi_{bo} - V - \Delta) - e/\epsilon_S \; N_{SS} \; X_o$$

now $\phi_s = -\Delta$

$$\therefore U_S = (\phi_o - \phi_S) = (\phi_{bo} - V - \frac{E_{CS}}{e}) - e/\epsilon_S \; N_{SS} \; X_o \qquad (7.29)$$

The surface state density N_{SS} is defined in equation (7.25) and substituting this into equation (7.29) we have

$$U_S = (\phi_{bo} - V - \frac{E_{CS}}{e}) - \frac{e X_o}{\epsilon_S} (N_S \sinh (C_2 U_S) + N_{SO})$$

$$\therefore U_S = (\phi_{bo} - V - C_S) - \frac{e X_o N_S}{\epsilon_S} \sinh (C_2 U_S) \qquad (7.30)$$

where $C_S = \frac{E_{CS}}{e} + \frac{e X_o N_{SO}}{\epsilon_S}$

which is an isothermal constant being dependent on the variation of the energy band levels in the semiconductor with temperature.

Equation (7.30) can be used to determine U_S using an iterative technique for a solution. This will then determine the barrier profile since N_{SS} can then be determined.

A graphical solution can be illustrated by rearranging equation (7.30) to the form.

$$\frac{\epsilon_S}{e X_o N_S} (\phi_{bo} - V - C_S - U_S) = \sinh (C_2 U_S)$$

The solution of U_S is then given by the point of intersection of the line,

$$\frac{E_S (\phi_{bo} - V - C_S - U_S)}{e X_o N_S}$$

with the curve $\sinh (C_2 U_S)$

This form of the solution for U_S is illustrated in figure 7.9 where indicated is the expected variation of U_S for a variety of conditions. It can be seen from equation (7.30) that U_S is a function of applied bias V so that the surface state density can be expected to vary with bias.

The zero bias condition is illustrated for the case of $(\phi_{bo} < C_S)$. It can be seen from the diagram that U_S will be smaller for positive bias than for forward bias. For the case of $(\phi_{bo} < C_S)$ then $U_S < 0$ for $V > -V_o$ where $V_o = (\phi_{bo} - C_S)$.

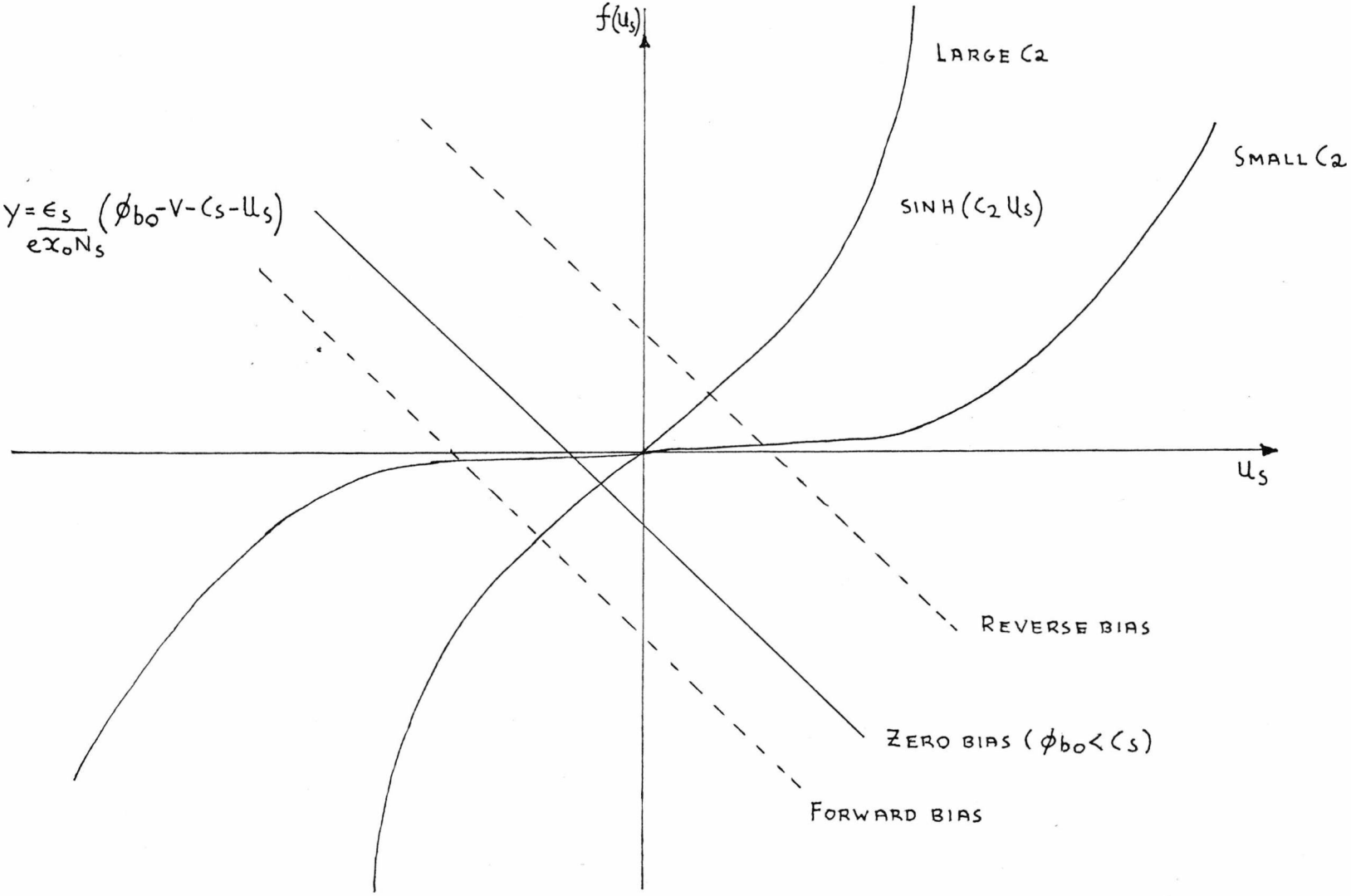


FIGURE 7.9 : VARIATION OF U_S WITH APPLIED BIAS .

If however $V < -V_o$ then $U_S > O$. It can also be deduced from the diagram that the variation of U_S will be very dependent on the density of surface state. U_S will vary to a lesser extent for large values of C_2, which implies a high density of surface states. Obviously in the extreme case ϕ_o will be pinned to ϕ_S at the surface of the semiconductor.

7.6. IMPLICATIONS OF THEORETICAL MODEL.

The implications of this theoretical model with respect to the current transport across metal-semiconductor interfaces can perhaps best be outlined by an analysis of the barrier profiles expected for the case of varying bias conditions. From figure (7.9) it can be seen that $N_{SS} > O$ for $U_S > O$ so that we can expect a barrier profile as shown in figure (7.10) for the case of reverse bias. This indicates that the effect of a positive surface charge is to provide a potential barrier with a sharp spike through which electrons may readily tunnel. This results in an effective barrier height which is less than ϕ_{bo}. If $N_{SS} >> O$ the spike may be so large that there is significant tunnelling from the electrons near the Fermi energy of the metal and a very large current will flow. This potential spike becomes sharper for the case $\phi_{bo} < C_S$ and for this reason we can expect the reverse bias characteristics for metal silicon contacts, involving a metal with a low work function, to be very soft. However, for the case $\phi_{bo} > C_S$ we can expect the reverse characteristics to be hard and there will be a breakdown condition when the reverse bias reaches the punch through voltage of the depletion region.

On the other hand the effect of a forward bias is to produce $N_{SS} < O$ with the implications that the barrier profile will be of the form shown in figure (7.11). From equation (7.19) and on the assumption that $W >> X_o$ so that $\exp - (\frac{W}{X_o}) = 0$ and $N_D (X_m - W) \rightarrow - N_o W$ it can be deduced that the barrier will have a maximum at

$$X_m = X_o \ln \left(\frac{-N_{SS}}{N_D W} \right) \qquad (7.31)$$

A more accurate solution can be obtained by an iterative solution of the equation.

$$N_D (X_m - W) - N_{SS} \exp \left(\frac{-X_m}{X_o} \right) = 0 \qquad (7.32)$$

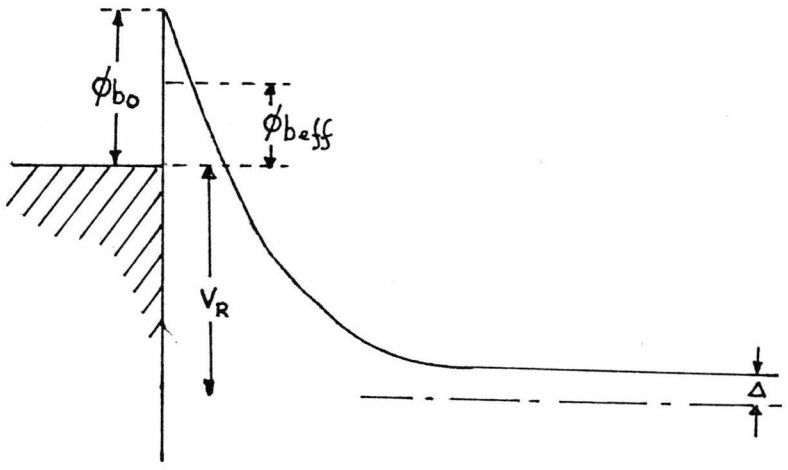


FIGURE 7.10 : REVERSE BIAS $V_R > V_o$

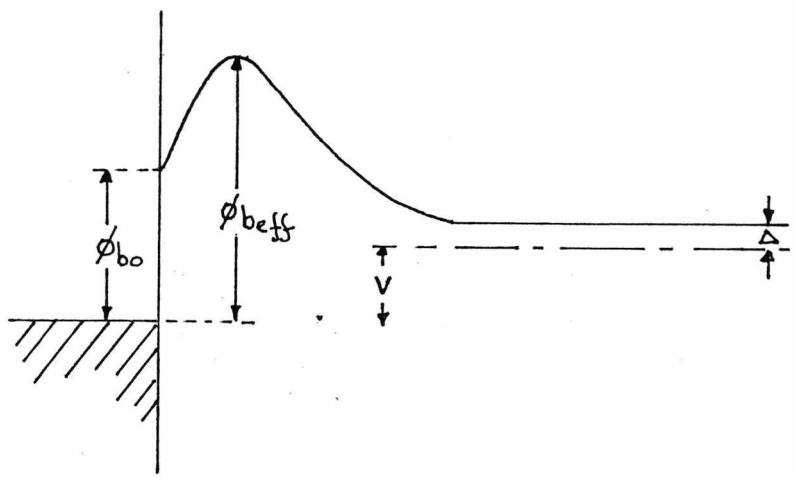


FIGURE 7.11 : FORWARD BIAS $V > -V_o$

The barrier maximum can then be determined from the potential distribution given in equation (7.20). In this case the effective barrier height $\phi_{beff} > \phi_{bo}$. Thus the current flow becomes relatively speaking more difficult so that the forward bias characteristics take the form,

$$J_f = J_o . \exp\left(\frac{eV}{nkT}\right) \text{ where } n > 1$$

Thus from similar considerations as applied to the reverse bias case, we can expect the value of n to vary to a certain extent with the value of metal work function being considered. These results can be summarised by a discussion of ϕ_{beff} as a function of applied bias and metal work function ϕ_m.

Figure 7.12 indicates the type of variation of ϕ_{beff} with applied bias that can be expected with varying values of ϕ_m. That is $\phi_m > 5.0$ eV and $\phi_m < 4.3$eV. This is typically the range of ϕ_m values that would be investigated in an analysis of metal-silicon contacts. For the case of low ϕ_m we can see that $\phi_{beff} > \phi_{bo}$ for the case of zero bias. ϕ_{beff} can be expected to decrease relatively rapidly with reverse bias. This effect will of course be dependent on the density of surface states N_S as $N_S > > _0$ will lead to a very large positive surface charge implying a large spike in the potential barrier. For this reason we can expect the largest variation of ϕ_{beff} with reverse bias for this particular case. For the case of forward bias ϕ_{beff} will increase relatively rapidly with applied bias thus implying a forward I - V characteristic far from the ideal.

For the case of high ϕ_m that is $\phi_{bo} > C_S$ we can expect $\phi_{beff} < \phi_{bo}$ at zero bias. For the case of reverse bias ϕ_{beff} will again decrease but this will not result in the large positive surface charge causing a thin potential spike as in the case for low metal work functions, due to the large value of ϕ_{bo} being considered. The forward bias condition will result in an increase of ϕ_{beff} so that non ideal characteristics are to be expected for this case as well. A sketch of the type of I - V characteristic that can be expected is illustrated in figure (7.13).

Considerations can now be given to the temperature variation that can be expected when analysing this theoretical model. The barrier profile and hence the I - V characteristics are basically dependent on the density of surface states N_{SS} which vary according to the value of U_S. We can therefore expect a certain temperature dependence of the barrier profile due to the variation of the Fermi level and band levels in the semiconductor. The Fermi level variation will lead to a variation of the value of U_S. The position of the Fermi level with the respect to the conduction band edge is given by,

$$\Delta = kT \log e \left(\frac{N_C}{N_D}\right)$$

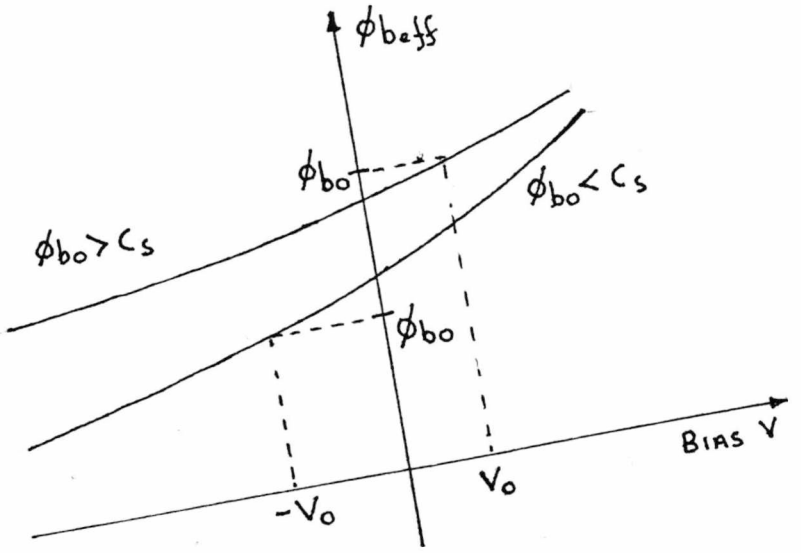


FIGURE 7.12 : ϕ_{beff} AS A FUNCTION OF BIAS

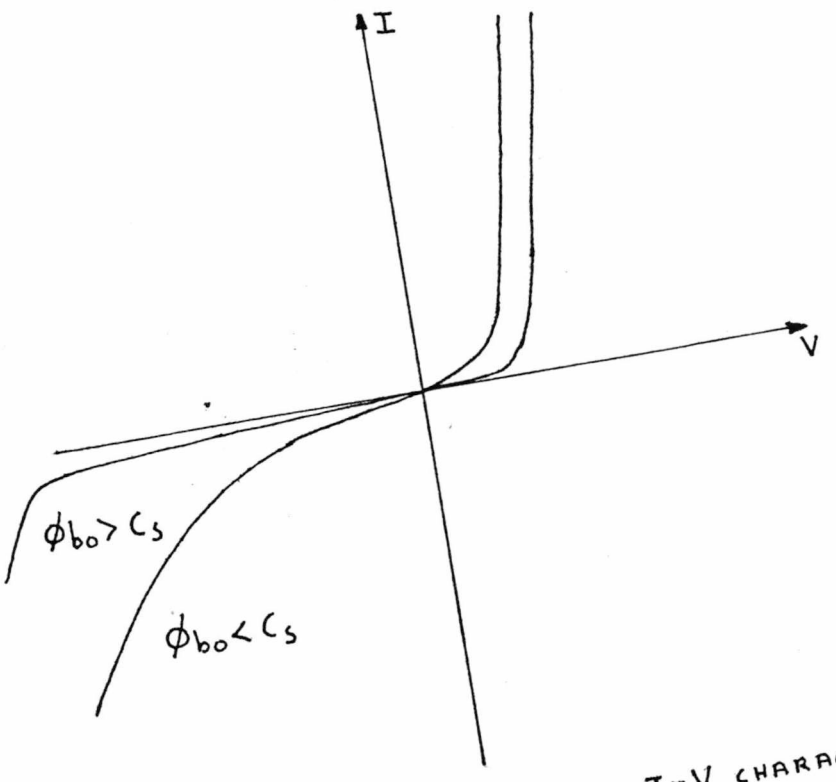


FIGURE 7.13 : THEORETICAL I-V CHARACTERISTICS

the value of N_C being also temperature dependent. The position of the Fermi level tends to the centre of the band-gap as the temperature increases. This type of temperature dependence on U_S can be seen to produce slight variation in the resultant barrier profile. If is difficult at this stage to guage the exact effects of temperature variation on the resultant barrier profile due to the complex nature of the equations, this however will become apparent when we consider the computations in Chapter 8.

However due to the strong influence of the surface state effects on the I - V characteristics we can expect the barrier heights obtained from C - V measurements to be quite different from thoseobtained from the I - V measurements. The effective capacitance is given by,

$$C = \epsilon_S / W \text{ per unit area}$$

where ϵ_S is the permittivity of the semiconductor and W is the depletion layer width. As larger reverse bias voltages is applied, the depletion layer expands as

$$W = 2\epsilon_S \frac{(V_D - V_R)^{\frac{1}{2}}}{e N_D}$$

and consequently the capacitance decreases

$$\therefore \quad \frac{C = A\ e N_D \epsilon_S}{2(V_D - V_R)}^{\frac{1}{2}}$$

where A is the sample area.

Qualitatively this result can perhaps best be understood in terms of the band diagram for intimate metal semiconductor contacts shown in figure 7.8. The intercept of a C^{-2} against V plot represents the diffusion potential $\left(V_D - \frac{kT}{e}\right)$ with the parabolic conduction band extrapolated right up to the metal-semiconductor interface. This barrier height is not therefore dependent on the effects of the surface states as $W >> X_o$ and for the case shown in figure 7.10 we can expect

$$\phi_{bC-V} > \phi_{beff}$$

Pellegrini [11, 12] in his analysis of metal-semiconductor contacts, based on the initial work of Heine, concluded that the barrier height values derived from C - V measurements should be higher than those obtained from I - V and photoelectric measurements.

Thus it can be seen from the preceding outline on the implications of the theoretical analysis that the situation tends to become rather complex,dependent on many parameters. It is therefore important to consider the theoretical analysis in the context of the experimental conditions. Previous analysis of metal silicon contacts have usually concerned chemically prepared surfaces inevitabi y involving an intermediate oxide layer. Hence this particular analysis does not become directly applicable with regards to most previous experimental work. The only known analysis involving intermediate metal silicon contacts has been based on surfaces prepared by cleaving under U.H.V. conditions. Thus it becomes most important when considering the experimental results to pay great attention to the expected characteristics from the theoretical model with regards to differing densities of surface states. Thus perhaps obtaining a degree of correlation between the experimental results and the various methods of surface preparation.

In the following chapter we apply the theoretical analysis directly to the experimental results obtained from the contacts formed during this work. Thus we can obtain valuable information with regards to the density of surface states involved when considering U.H.V. heat cleaned surfaces. Thus a direct comparison can be made with the results obtained from U.H.V. cleaved silicon surfaces where a higher density of surface states is to be expected.

CHAPTER 8

CONCLUSIONS

8.1. ANALYSIS OF RESULTS

The data obtained from the experimental results can now be evaluated with respect to information derived from the theoretical model. Consideration must be given with respect to the various values used for the parameters related to the effects of the metal quantum tails decaying into the silicon band structure.

A value of $3A^{\circ}$ was used for the mean penetration depth of the metal quantum tails, this being the value deduced by Heine[6] and also the value computed in the analysis of intimate metal-semiconductor contacts, for the case of silicon, performed by Louie, Chelikowsky and Cohen[15]. In their detailed theoretical analysis of the electronic behaviour at the interface, states similar to those proposed by Heine[6] were determined. These states being referred to as metal Induced Gap States (MIGS). Figure 8.1 indicates the distribution of these surface states in the silicon band gap computed during their work. This computation for the distribution of the surface states was used as a basis in order to determine the values for C_2, N_S, N_{SO} and the position of the neutral level to be used in the theoretical analysis (see equation 7.23). Fitting this distribution to the form of equation (7.21) values of $C_2 = 2$ and 0.35eV for the position of the neutral level above the valence band are obtained when considering the boundary conditions. However N_S and N_{SO} are the parameters of most interest when considering the theoretical analysis. Given the potential distribution in equation (7.20) it is possible to obtain the optimum values for N_S and N_{SO} from the experimental results for each metal-silicon contact type.

To this end the work of Nahab[92] has been used since he provided a comparison of the various methods of data interpretation with particular reference to the case of metal-semiconductor contacts. The method that he recommends is to optimise values of parameters by a least square fit to the experimental data and he shows that a procedure based on the work of Marquardt[93] is suitable for this purpose.

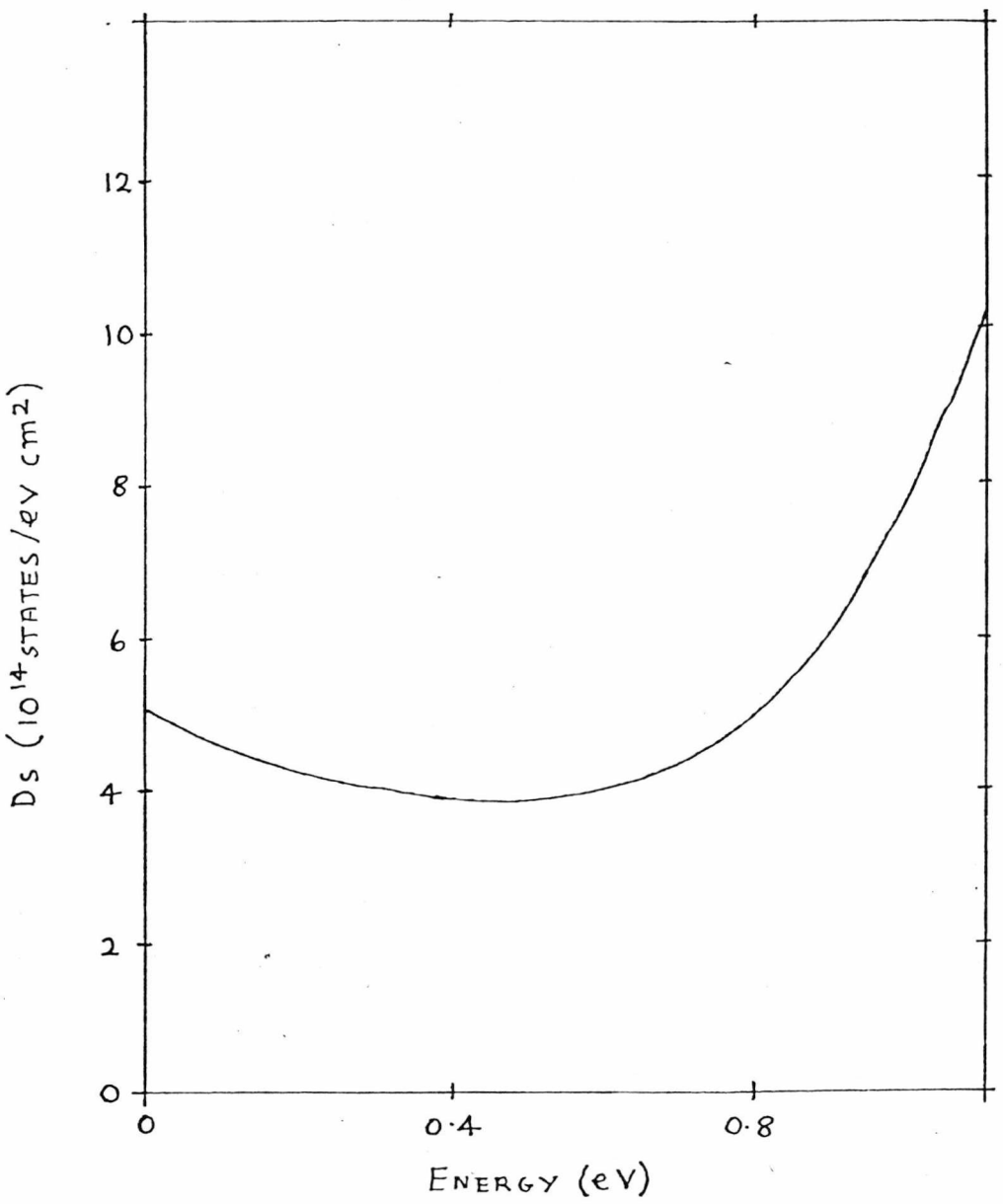


FIGURE 8.1 : SURFACE DENSITY OF STATES.

In order to explain this procedure it is necessary to consider the set of parameters to be determined as a matrix X, i.e.

$$X = \{N_S, N_{SO} \quad ----\}$$

Thus for this particular work we are interesting in obtaining values for the surface state parameters N_S and N_{SO}.

A theoretical form of current flow can be found for any values of the independent variables V, T. Thus it is possible to determine the theoretical current flow I_T (V_i, TK) where j and k are integers which label the particular measured experimental value I_E (V_i, T_K). It is therefore possible to treat the data as a number of isotherm al sets so that any temperature dependence should become apparent.

The objective is now to determine the optimum set X for each temperature. This is achieved by minimising the function

$$S = \frac{1}{n} \sum_{j=1}^{n} \left\{ \ln (I_T/I_E) \right\}^2 \qquad (8.1)$$

where n is the number of voltage points at a particular value of K. It is clear that S is minimised if

$$\frac{\partial S}{\partial x_i} = 0 \qquad (8.2)$$

where x_i represents the i^{th} parameter of the set X to be found. Equation (8.1) represents p simultaneous equations where p is the number of parameters to be optimised. Thus it is possible to use equation (8.1) in order to determine each of the parameters but there is however the problem that the equations are non-linear and transcendental so that an iterative technique will be required. Nahab shows that equation (8.2) can be solved by the use of a multi dimensional Newton-Raphson approach with the gradient being automatically adjusted in order to avoid instabilities. The formulation becomes

$$X = X_o - \left[ZZ^T (1 + \lambda_1) I + \lambda_2 I \right]^{-1} \left[Zf \right]$$

in which X_o is an initial estimated set of X and Z is the Jacobianmatrix defined by

$$Z = \begin{bmatrix} \frac{\partial f}{\partial X_1})_1 & \cdots & \frac{\partial f}{\partial X_i})_1 & \cdots & \frac{\partial f}{\partial X_p})_1 \\ \vdots & & \vdots & & \vdots \\ \frac{\partial f}{\partial X_1})_i & \cdots & \frac{\partial f}{\partial X_i})_i & \cdots & \frac{\partial f}{\partial X_p})_i \\ \vdots & & \vdots & & \vdots \\ \frac{\partial f}{\partial X_1})_n & \cdots & \frac{\partial f}{\partial X_i})_n & \cdots & \frac{\partial f}{\partial X_p})_n \end{bmatrix}$$

Z^T is the transpose of Z, I is a unit matrix, and λ_1, λ_2 are parameters used in order to preserve stability. The matrix $[f]$ is a columnmatrix defined by

$$[f] = \begin{bmatrix} \ln \left({}^{I}T_1 / I_{E_1} \right) \\ \vdots \\ \ln \left({}^{I}T_i / I_{E_i} \right) \\ \vdots \\ \ln \left({}^{I}T_n / I_{E_n} \right) \end{bmatrix}$$

The value of λ_2 is made small but finite and is used to avoid computational overflow when the gradient $[ZZ^T]$ is small. This corresponds to starting the Newton-Raphson technique close to a turning point in the function $(\partial S / \partial x_i)$

It may also be anticipated that problems will occur if the iteration extrapolates to values of X that are outside reasonable physical limits, that is the step from X_o become too large. Under these circumstances non-zero values of λ_1 will reduce the step, indeed as λ_1 increases then the step will decrease. Thus the procedure adopted uses integral values of λ_1 which are increased as a result of parameters being outside reasonable physical limits. When a valid set of X has been determined then λ_1 is reset to zero in order to provide the maximum convergence.

The basic software package for this form of computation was available it only being necessary to introduce the parameters to be determined.

The theoretical current flow being considered in terms of the thermionic component and that due to quantum mechanical tunnelling. The results obtained for the metal-silicon contactsare shown in figure (8.2). It is possible to use this information in the theoretical model in order to establish the validity of the theoretical approach. A Fortran programme was written to this effect to run on a mini-computer. The various theoretical equations derived in Chapter 7 were used in order that the relevant information such as depletion layer width, value of U_S and N_{SS} could be determined under varying bias and temperature conditions. These values can then lead to a computation of the barrier height, by the use of the theoretical equation for the barrier profile in conjunction with the expression for the position of the barrier maximum.

All the equations used in this computer model are given in Chapter 7, however perhaps the best method of outlining how these are used in order to determine the various parameters is by considering the flow chart in figure 8.3. This flow chart indicates the basic software blocks in the computer programme, POT(x) being a function subroutine calculated from the equation of the barrier profile presented in Chapter 7.

Initially the values of kT, E_G, N_C and Δ are determined for the particular temperature. N_C being the density of states in the conduction band and being proportional to $T^{3/2}$. Δ is then given by,

$$\Delta = kT \ln (N_C/N_D)$$

From the density and distribution of surface states information, U_S can be determined by the use of a iterative technique from equation (7.30). The depletion layer width W can then be determined from equation (7.28). Again aniterative technique can be used in order to calculate the position of the barrier maximum X_m from equation (7.32). These calculated values can then be used in equation (7.20), for the potential distribution in the depletion layer, in order to determine a theoretical value for the barrier height.

The other data input required for this model is obviously values for the metal work functions and for the electron affinity of silicon. A value of 4.05 eV for the electron affinity of silicon was used due to the fact that this value has consistently been measured in the majority of recent experimental work. The values used for the metal work functions were obtained from the experimental results reported by Thonalikis[34] from U.H.V. in stitu measurements on freshly deposited metal films. These values being in good agreement with the values selected by Riviere[116] to be the most representative from published data. It is thus hoped that the values used are the most applicable to the case being considered taking into account the most accurate data available at present.

METAL	EPITAXIAL LAYER		HEAT CLEANED	
	$N_S \times 10^{13}\ cm^{-2}$	$N_{SO} \times 10^{13}\ cm^{-2}$	$N_S \times 10^{13}\ cm^{-2}$	$N_{SO} \times 10^{13}\ cm^{-2}$
Au	4·4 ± 0·1	-5·9 ± 0·1	4·5 ± 0·1	-6·0 ± 0·1
Cr	4·1 ± 0·1	-6·05 ± 0·1	4·05± 0·1	-6·1 ± 0·1
Ag	4·2 ± 0·1	-5·9 ± 0·1	4·1 ± 0·1	-6·05 ± 0·1
Al	4·0 ± 0·1	-6·0 ± 0·1	4·05 ± 0·1	-6·1 ± 0·1

FIGURE 8.2 : VALUES DETERMINED FOR N_S AND N_{SO}.

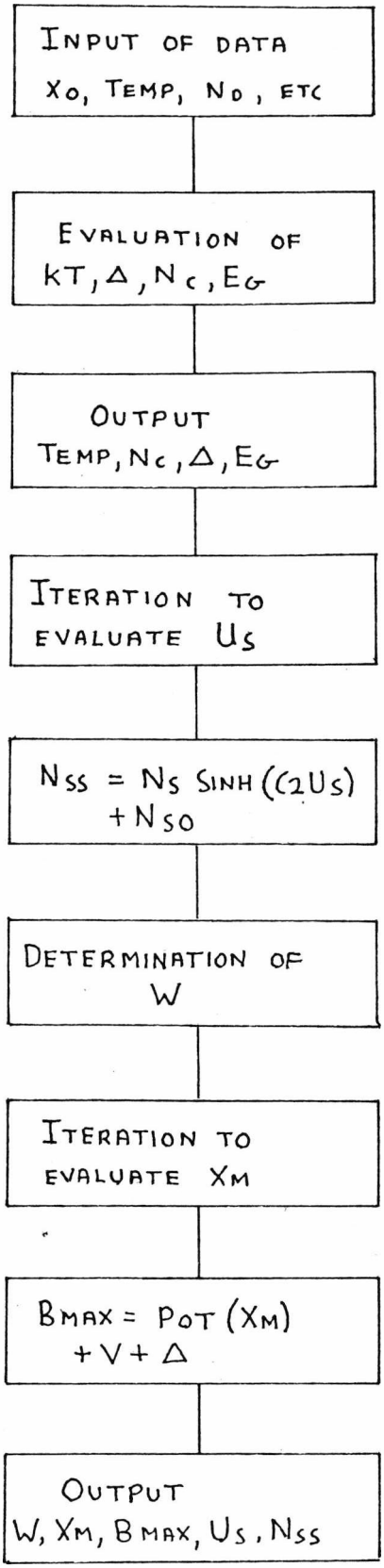


FIGURE 8.3 : FLOW CHART OF THEORETICAL MODEL

Errors concerned with the various input data to the model can be run through the programme in order to determine the errors involved with the output information obtained. The computer programme was run for all the metals investigated over the temperature ranges used during the experimental work.

Figure 8.4 is a table of the experimental results obtained for the zero bias, barrier heights listed with the corresponding data obtained from the theoretical computer model. Also listed in this table are the results reported by Thanalikis[39] for the case of intimate contacts formed onto U.H.V. cleaved silicon surfaces. It can be seen that when considering the errors in volved in both the experimental results and the theoretical data, in general good agreement has been obtained for all the contacts being considered. It is however immediately apparent that there are considerable discrepancies when considering the data for the cleaved surfaces and this will be discussed shortly.

Figure 8.5 is a graph of the measured barrier heights against the value of metal work function, the results for the cleaved surfaces also being ploted. It is apparent that neither of these plots are linear and this is not surprising in the light of the type of surface state distribution being considered. The results for barrier heights obtained during this work are substantially lower than the results reported by Thanalikis[34] with the exception of Gold, certainly outside of what one might consider to be experimental error. This discrepancy would not seem unreasonable in the light of the significantly higher density of surface states reported for cleaved surfaces[16]. Also other considerations related to these differing results are discussed in the next section. It was apparent, from results obtained from the computer model, that considering higher densities of surface states would certainly tend towards the results reported for the cleaved surfaces, and eventually the barrier height will become totally dependent on the position of the neutral level in the silicon band-gap.

With all these points in mind the pure evaluation of results in terms of zero bias barrier heights is perhaps not the most informative, as different values used in the same theoretical model can be seen to produce results similar to those obtained from the cleaved surfaces. However, the temperature dependence of barrier height and more important the variation of barrier height with bias can be seen to provide more information as to the validity of the proposed theoretical model. This being due to the substantial bias dependency of the barrier profile in the computer model, as discussed in Chapter 7.

METAL	WORKFUNCTION ϕ_m eV	BARRIER HEIGHT EPITAXIAL LAYER eV	BARRIER HEIGHT HEAT CLEANED eV	BARRIER HEIGHT CLEAVED eV	BARRIER HEIGHT THEORETICAL eV
Au	5·10 ± 0·05	0·83 ± 0·005	0·83 ± 0·005	0·73 ± 0·005	0·82 ± 0·02
Cr	4·47 ± 0·05	0·68 ± 0·005	0·69 ± 0·005	—	0·67 ± 0·02
Ag	4·41 ± 0·05	0·63 ± 0·005	0·64 ± 0·005	0·68 ± 0·005	0·64 ± 0·02
Al	4·17 ± 0·05	0·49 ± 0·005	0·50 ± 0·005	0·61 ± 0·005	0·51 ± 0·02

FIGURE 8.4 : ROOM TEMPERATURE BARRIER HEIGHTS

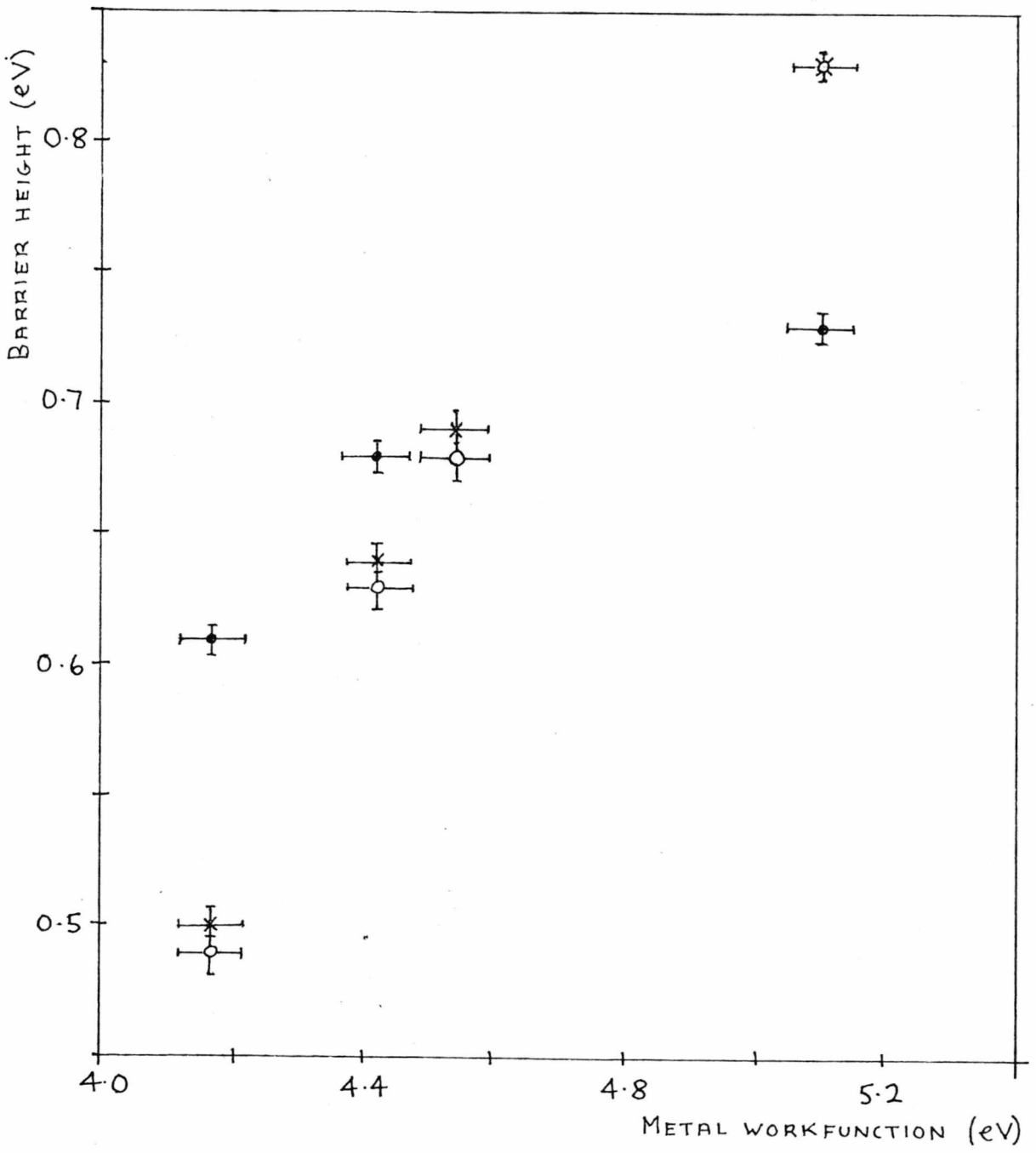


FIGURE 8.5 : ϕb v ϕm

• CLEAVED
X HEAT CLEANED
o EPITAXIAL LAYER

Figure 8.6 to 8.9 show the variation of barrier height with temperature in comparison with the data obtained from the theoretical model for all the contacts being considered. It can be seen that there is good agreement with the type of variation expected from the model. The departures certainly within the errors being considered. However a wider temperature range may have been more useful for a better comparison. It is interesting to note that these results are in good agreement with the type of variation reported for good cleaved surfaces[33] and not the more dramatic variations reported for poorly cleaved surfaces.

The variation of barrier height with bias is perhaps the most significant parameter in this analysis of results. This information must now be obtained from the theoretical model. From the theoretical analysis in Chapter 7 it can be shown that

$$\phi_{beff} = \psi(Xm) + V + \Delta \qquad (8.3)$$

where $\psi(Xm)$ is the potential at the barrier maximum, Δ the position of the Femi level relative to the conduction band edge in the bulk semiconductor and V the applied bias.

$$\psi(Xm) = \frac{e}{\epsilon_S}\left[N_o \frac{(W - Xm)^2}{2} + N_{SS} X_o \exp\frac{(-X_m)}{X_o}\right] \qquad (8.4)$$

We must therefore determine $\frac{\partial \psi(X_m)}{\partial V}$ for all the temperature ranges investigated.

For this purpose the following equations derived in Chapter 7 will be required.

$$N_{SS} = N_S \sinh(C_2 U_S) + N_{SO} \qquad (8.5)$$

$$W = \left[2\epsilon_s \frac{(\phi_{b0} - V - \Delta)}{eN_o} - \frac{2N_{SS} X_o}{N_o}\right]^{\frac{1}{2}} \qquad (8.6)$$

$$X_m = X_o \ln\left(\frac{-N_{SS}}{N_o W}\right) \qquad (8.7)$$

$$U_S = (\phi_{bo} - V - C_S) - e\frac{X_o N_S}{\epsilon_S}\sinh(C_2 U_S) \qquad (8.8)$$

It however can be seen from this analysis that the variation of barrier height with bias will not be a linear function, due to the fact that the variation of surface charge with bias is not linear. However considering small bias conditions this will be sufficiently linear to allow the approximation as below.

$$\sinh(C_2 U_S) \simeq C_2 U_S$$

Also the experimental data was interpreted on the basis of a linear function. Examination of the log current versus voltage plots in Chapter 5 do however indicate only small departures from this linear approximation over the forward bias range being considered.

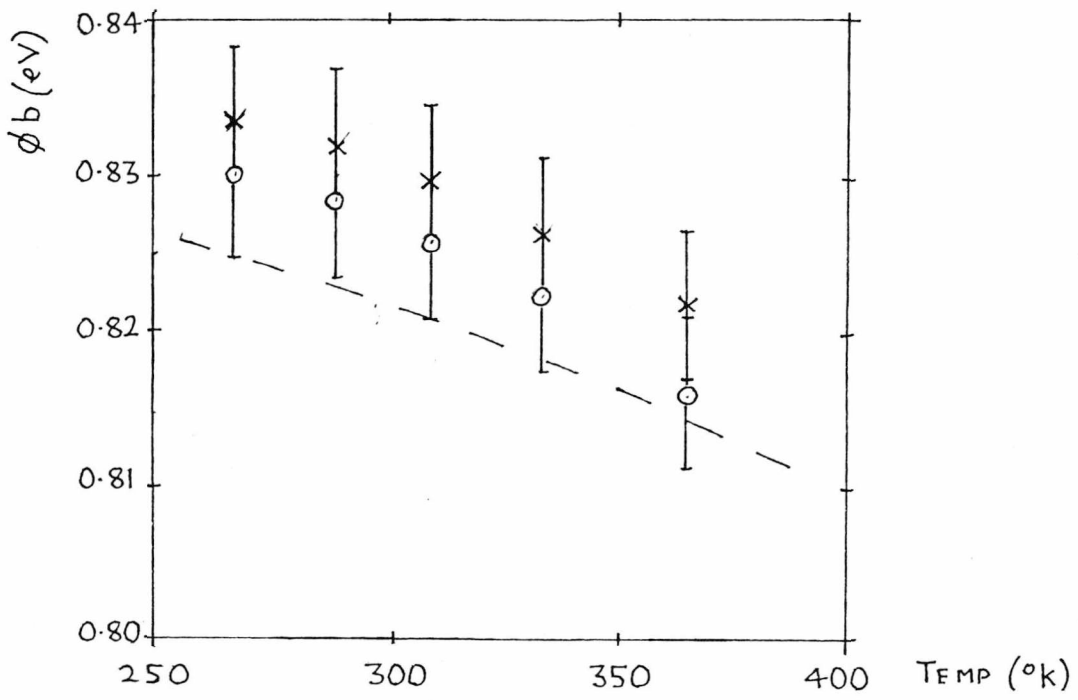


FIGURE 8.6 : Øb V TEMP

× AU - SILICON (HEAT CLEANED)

o AU - EPITAXIAL LAYER

--- THEORETICAL

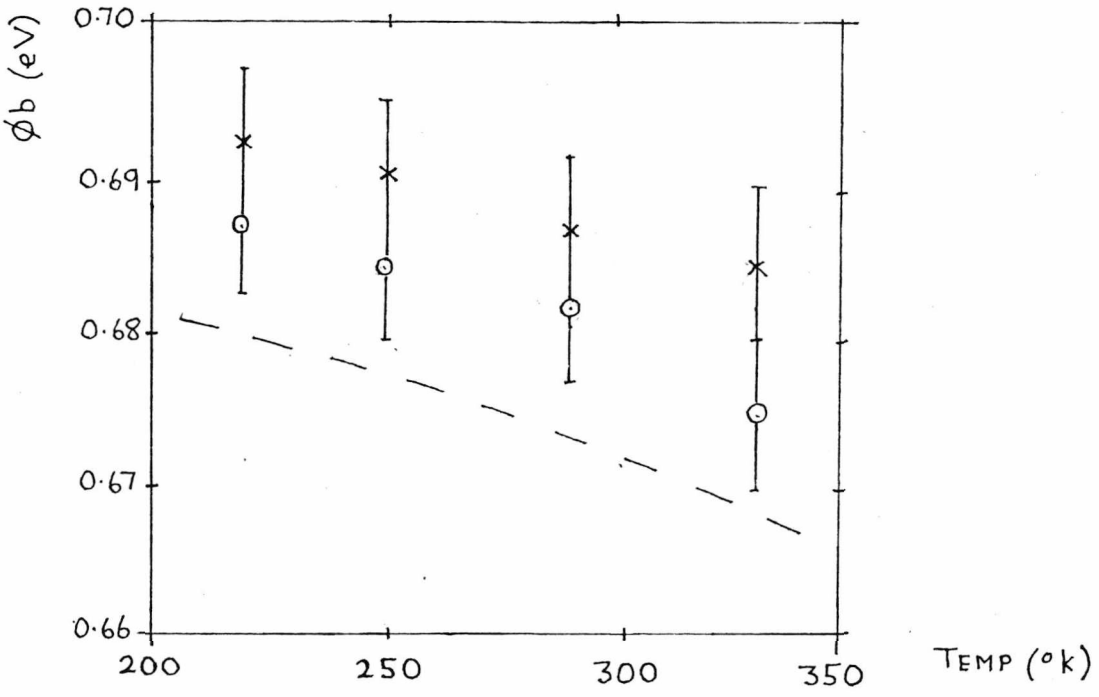


FIGURE 8.7 : Øb V TEMP

× Cr - SILICON (HEAT CLEANED)

o Cr - EPITAXIAL LAYER

--- THEORETICAL

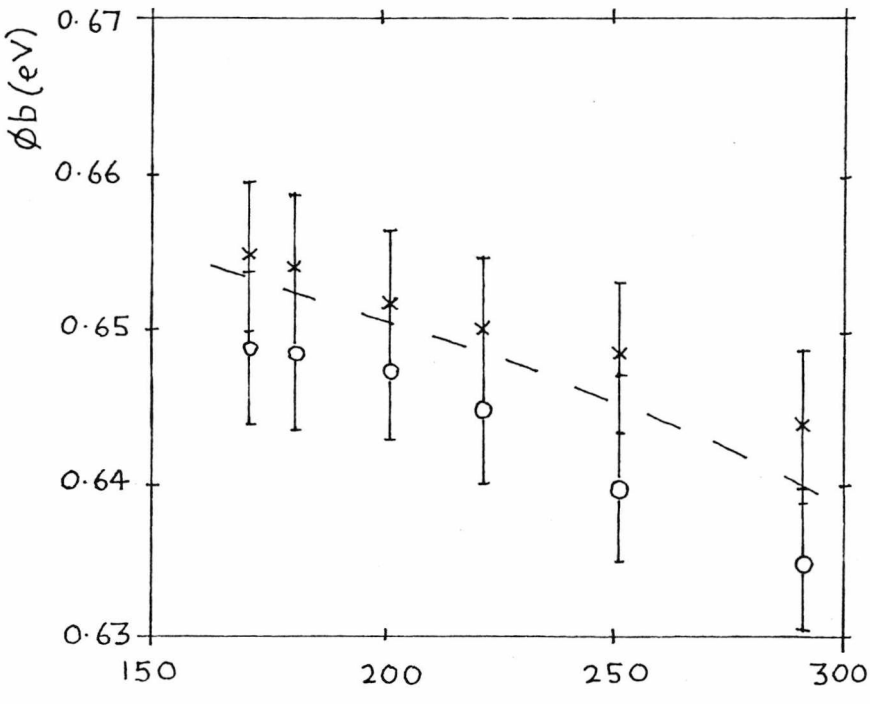


FIGURE 8.8 : Øb V TEMP

× Ag - SILICON (HEAT CLEANED)

o Ag - EPITAXIAL LAYER

--- THEORETICAL

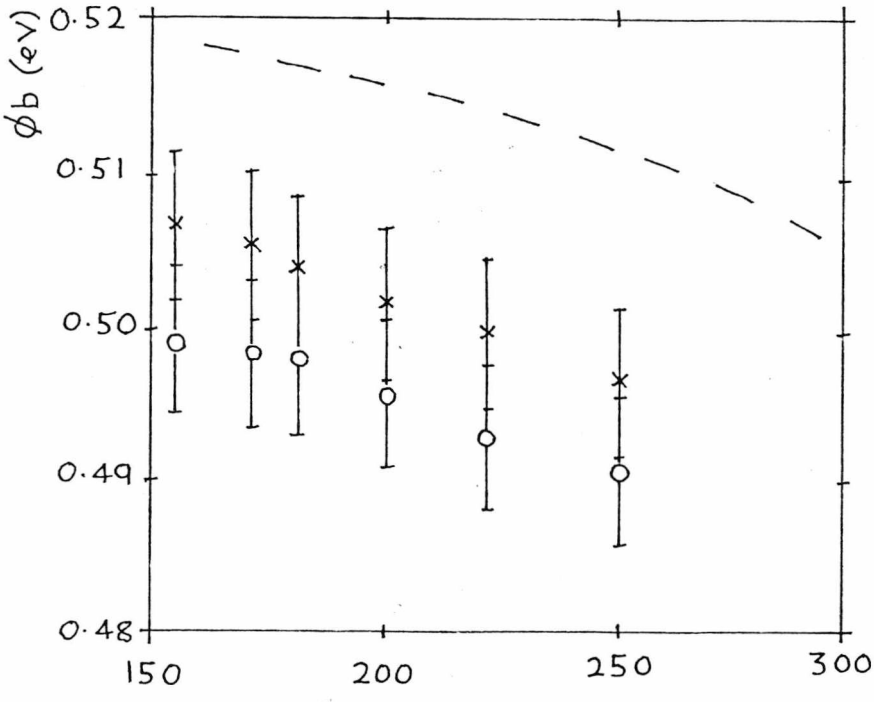


FIGURE 8.9 : Øb V TEMP

× Al - SILICON (HEAT CLEANED)

o Al - EPITAXIAL LAYER

--- THEORETICAL

A computer programme was written, from these various equations, in order to determine theoretical values for the variation of barrier height with bias. This was achieved by calculations of the dominant terms when considering equations (8.5) to (8.8) in the expression for the barrier maximum. Thus data could be obtained for the metal silicon contacts being considered over the required temperature range. It soon becomes apparent however that the theoretical variation of barrier height with temperature is not a significant factor. This data can be compared with the experimental values obtained from the data interpretation in Chapter 6. Figures 8.10to 8.13 indicate the variation of this parameter over the temperatures ranges investigated. A comparison of this barrier height variation with temperature would seem to be a very useful means for evaluation of the theoretical approach. These diagrams indicate good agreement in general between the experimental and theoretical values. However, there are definitly discrepancies noticeable at the lower temperature measurements. This would tend to suggest that there is present a temperature dependent mechanism in the current transport at the interface. However, from the magnitude of the departure from the theoretical model it can be concluded that this mechanism cannot be considered to be dominant at the temperatures involved, thus giving support to the type of data interpretation employed during this work.

Thus the results from the intimate metal-silicon contacts give good support to concepts used in the theoretical model, with also good agreement being obtained between the two contacts types investigated during this work.

8.2. DISCUSSION

The object of this section is to try and draw together the most important information obtained from previous investigations into metal-silicon contacts thus being able to put the various results obtained during this research work in perspective with the available data from other research work. The section also acts as a kind of summary to the work undertaken.

In all previous experimental analysis of metal-silicon contacts only two basic methods of the formation of the contact have been given any real consideration. Vaccum heat cleaning under U.H.V. conditions has not previously been considered practical for metal-silicon contact analysis mainly due to the fact that most previous

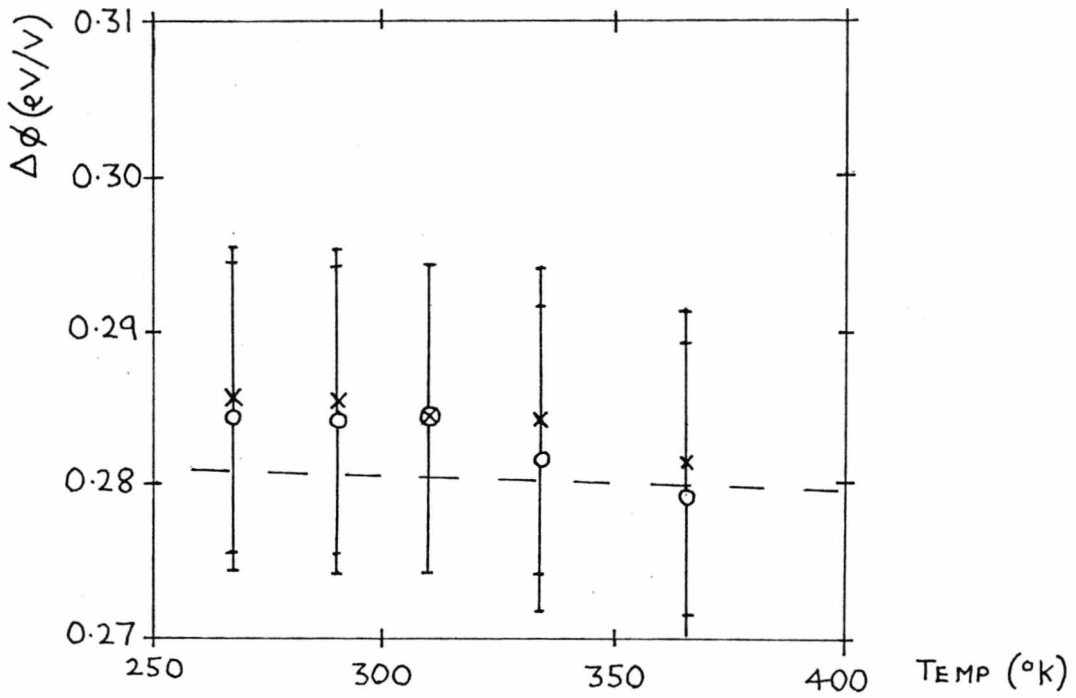


FIGURE 8.10: Δφ V TEMP

x Au-SILICON (HEAT CLEANED)

o Au-EPITAXIAL LAYER

--- THEORETICAL

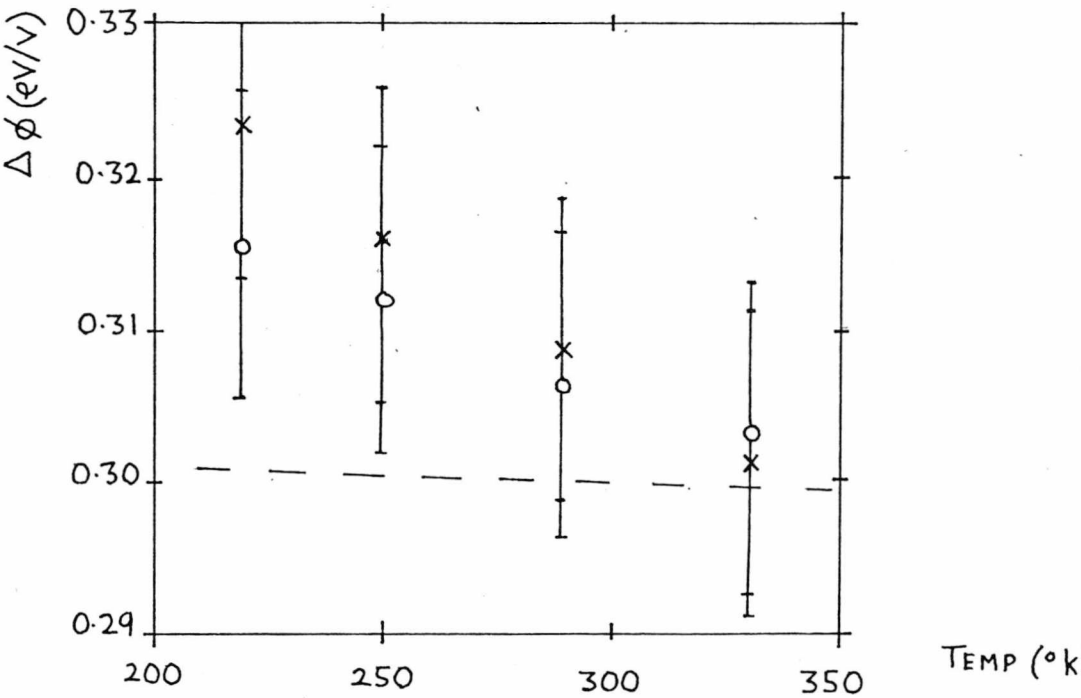


FIGURE 8.11 : Δφ V TEMP

x Cr- SILICON (HEAT CLEANED)

o Cr- EPITAXIAL LAYER

--- THEORETICAL

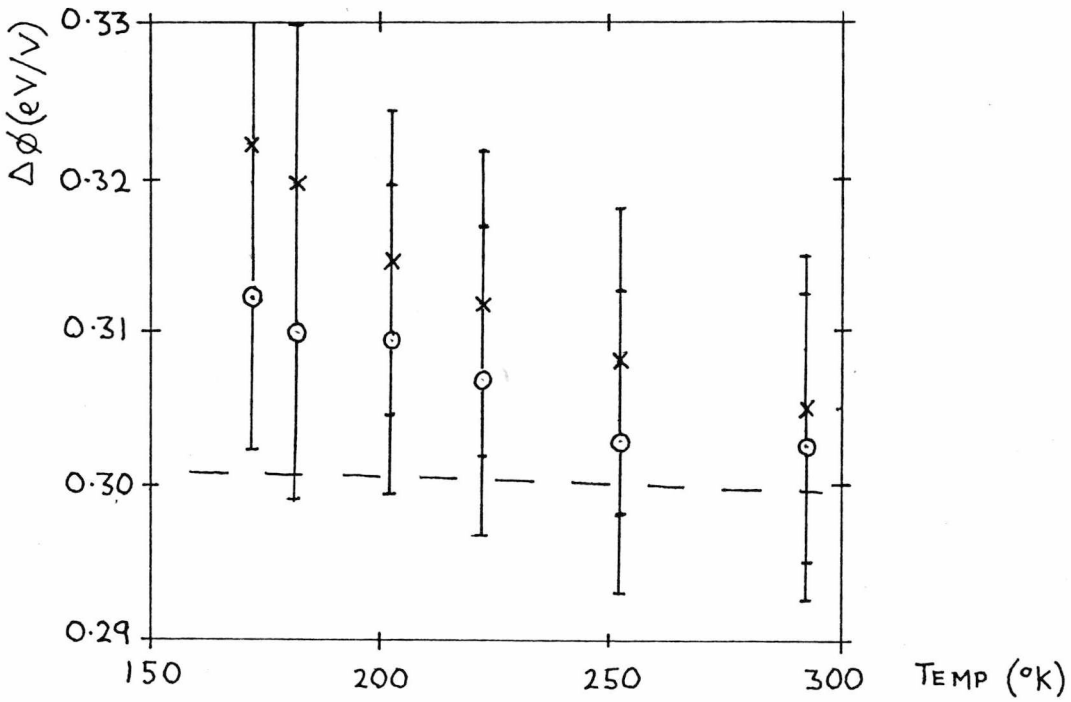


FIGURE 8.12: Δφ V TEMP

× Ag-SILICON (HEAT CLEANED)

o Ag-EPITAXIAL LAYER

--- THEORETICAL

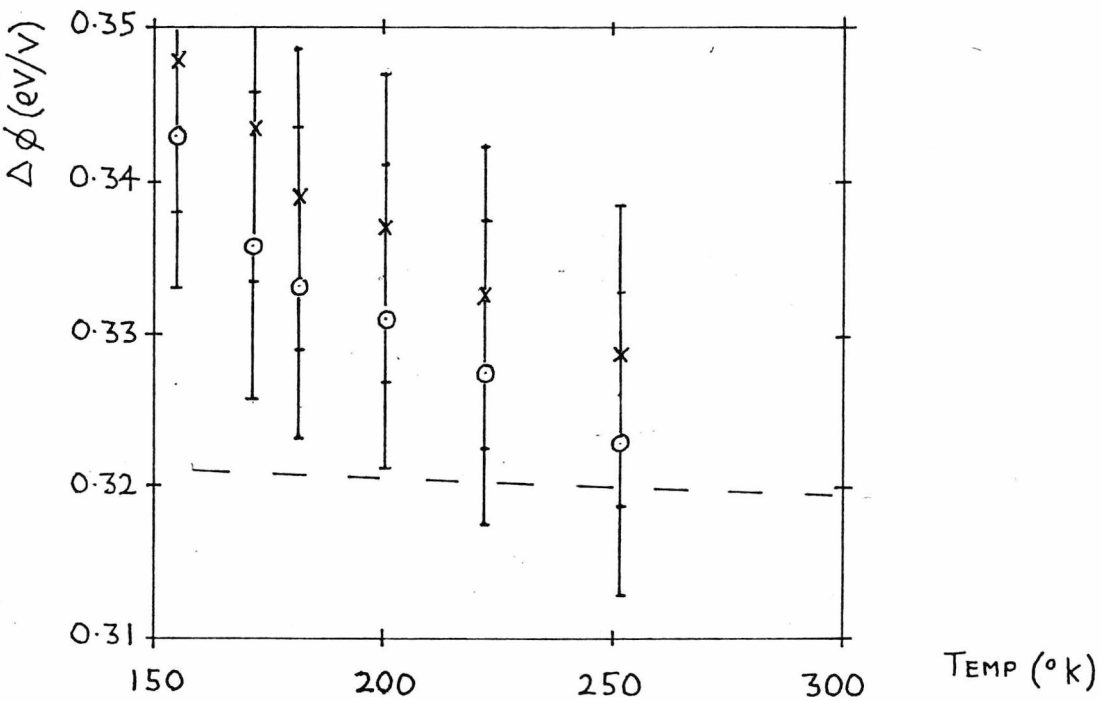


FIGURE 8.13: Δφ V TEMP

× Al-SILICON (HEAT CLEANED)

o Al-EPITAXIAL LAYER

--- THEORETICAL

attempts at this technique have lead to the formation of a p-type surface layer[77,117,118] presumably caused by some Group III impurity being present in the vacuum system. This effect was discussed in the review of cleaning techniques in Chapter 3.

For the majority of experimental research work some form of chemical cleaning preparation of the silicon surface has been undertaken prior to the deposition of a metal film under varying vacuum conditions. It is of course always possible that there may still exist some form of contamination after particular chemical cleaning procedures, perhaps even caused by the use of the chemicals themselves. It would appear from a study of the literature[5,16,81] that there exists a wide range of reported I-V characteristics and barrier height values for metal silicon contacts formed in this manner. One could therefore easily conclude that the surface preparation and the subsequent conditions under which the metal contact is formed play a dominant role in the ultimate electrical characteristics of the devices so formed. In practice a metal silicon junction formed in this manner will inevitably include a thin insulating layer of oxide between the metal and semiconductor. The thickness of this interfacial layer is dependent on both the exposure time of the silicon surface to atmospheric conditions and the manner in which the first layer of metal atoms sits on the semiconductor surface. It would seem reasonable to assume that a value for this interfacial layer thickness varies by ±50% about some mean value. Thus it is perhaps not surprising, from the various considerations outlined in Chapter 7, that the variations in the thickness of this interfacial layer in conjunction with the effects of the various chemical preparations on the nature of the silicon surface will inevitably lead to differing experimental results reported for the barrier heights. The interfacial layer is normally so thin ($\sim$ 10 A^{o}) that electrons can tunnel through it quite freely, but it is of course of importance due to the role this layer plays on the effects of the silicon surface states.

From a study by Turner and Rhoderick[16] it would appear that there is some form of ageing process involved with contacts where an interfacial layer is known to be present. This would seem to be associated with a slow change in the thin oxide film leading to a gradual variation of the measured barrier height with time until an equilibrium state is reached. This time period to reach equilibrium would seem to be dependent on the surface preparation. It is interesting to note that widely differing results for various surface preparations tend to converge to near one value when this ageing process is complete. This ageing process may be attributed to the migration

of charged ions through the oxide. The effects of these charged ions would disappear when they reached the metal and their charge was neutralised. Thus considering all these factors and the range of reported experimental results it would appear that metal silicon contacts cannot be understood in any great depth from a study of chemically prepared surfaces as far too many external influences mask the true nature of the contact. As regards to the data interpretation methods applied to the results obtained from these contacts; many of the experimental workers always tried to fit the experimental barrier heights obtained if not to the Schottky relationship then to some form of linear relationship with the values of metal work function. This could tend to lead to misleading conclusions being drawn from the data also as in many cases doubtful values of metal workfunctions were used.

For the case of many results reported for cleaved silicon surfaces there will be present an interfacial layer. Since the residual pressure in the vacuum system can be as high as 10^{-7} to 10^{-6} torr for many of the reported experiments[5] a monolayer can form on the cleaved surface in less than one second to a few seconds depending on the sticking coefficient of the residual gases[5].

When considering cleaved silicon surfaces under U.H.V. conditions, it has been shown that there is a tendency of the barrier heights measured to be virtually independent of the metal used. This can be explained in terms of higher densities of surface states being present. However, perhaps the most concerning aspect of this technique is the surface nature of the silicon after it has been cleaved. The surface nature of cleaved silicon was discussed in Chapter 3, we must however consider the consequences on the electrical properties of metal silicon contacts formed by this technique. Evidence presented in the literature[16] indicates strongly that the electrical characteristics and hence the barrier heights are very dependent on the quality of the cleaved surface. This dependence on the nature of the surface after cleavage has been investigated by Van Otterloo and de Groot[33]. From I-V measurements it was determined that the barrier height was voltage dependent and the reverse bias characteristics were found to be soft It is interesting to note that these effects become more pronounced for the case of a bad cleavage. It should however be mentioned that the silver silicon contact was the only one being considered in this work. However a full analysis from the I - V measurements was not considered due presumably to the lack of information with regards to the nature of the barrier profile under differing bias conditions. This does tend to

give support to the type of data interpretation technique used during this work and explained in Chapter 6. Van Otterloo and de Groot employ the basic thermionic emission model with allowance for image force lowering. This indicates that the usual consideration of an ideality factor is just not adequate when trying to consider a full analysis of intimate metal-silicon contacts. One interesting point arrising from the C-V measurements that were undertaken in their work was that the barrier height determined were substantially lower when considering a poorly cleaved surface. This would tend to suggest a more profound difference on the nature of the contact rather than just considering different densities of surface states. The temperature variation of barrier height when considering a poor cleaved surface correlates with a certain degree with the surface state model proposed by Allen and Gobeli [115]. This substantial variation in electrical properties with quality of cleavage would tend to support the view that the electron affinity of the silicon can vary under differing surface conditions. This view can perhaps be substantiated in terms of the exposure of different surface orientations. In fact experimental investigations on vacuum cleaved silicon surfaces[119] has indicated a variation of electron affinity dependent on the quality of cleavage and values from 4.01 eV to 3.75eV have been obtained. This of course leads again to the consideration of the different surface strudures one can expect for cleaved surfaces compared to thermally cleaned surfaces[38]. These variations are also reflected in the values used for the electron affinity of silicon in previous data interpretation methods. Rhoderick and Turner[16] use of value of 3.75eV in their analysis involving cleaved surfaces. This one might consider to be on the low side especially without any clear substantiation. Also at this time the value of the work function for Gold was under considerable doubt with the value rising from 4.7eV to above 5.0eV. In fact it can be seen that most recent attempts of analysis of metal semiconductor contact data tend to lead to oversimplified conclusions. This can be attributed to the lack of importance placed on the surface preparation, the values used for various metal work functions and perhaps principally the inadequate methods used in order to interpret the data obtained. Thanallkis[34] uses a value of 4.85eV for the work function of silicon which is in agreement with the work of Allen and Gobeli[115] perhaps indicating this is a true value for cleaved surfaces. The work of Thanalikis[34] has lead to the formation of intimate metal-silicon contacts but important consideration must be given to the nature of the silicon surface in question.

The widely differing electrical properties that have been shown to exist for contacts formed onto differing quality cleaved surfaces tend to support the view that this is not the most reliable technique.

In this present work two techniques have been considered for the attainment of a silicon surface suitable for a study of intimate metal to clean silicon contacts in which the nature of the surface is of prime importance. There is strong evidence to suggest that the growth of an epitaxial layer by sublimation under U.H.V. conditions[36,71] will produce a surface suitable for this work. This being basically due to the fact that we have in this technique the ability to produce a good quality fresh silicon layer in the U.H.V. chamber immediately prior to the deposition of the metal film. A technique of U.H.V. heat cleaning of the silicon surface was employed to produce a surface suitable for subsequent epitaxial growth as well as a means in its own right to produce the surface required for the formation of an intimate metal clean silicon contact. This technique has been used extensively for the preparation of surfaces suitable for subsequent epitaxial growth[71,72,74-76]. During work carried out to this aim much experimental evidence [36,45,68-70] has built up to substantiate that this technique does in fact produce a clean non impurity stabilised silicon surface. The fact that good quality epitaxial layers have been grown using this technique must tend to support this view. U.H.V. heat cleaning has been investigated in full by Gale[36] and his recommendation of 5 minutes at 1200°C to be the most optimum was used during this work. The only main doubt raised with regards to metal-silicon contact formation was the observance of the formation of a P-type surface layer[77] which was not encountered during this research work. The metal film was deposited immediately after the heat cleaning procedure or the growth of the epitaxial layer had been terminated. Thus considering the pressure at which this operation was performed ($\sim 5 \times 10^{-9}$ torr) the possibility of an interfacial layer being able to form can be considered minimal. The device formation technique, after the actual interface had been produced, hopefully minimising any other contamination effects.

The I-V measurement system was designed in order to produce an environment in which the most accurate results could be obtained under stable conditions.

Good correlation has been observed from all the data obtained from the contacts involving the heat cleaned surfaces and the contacts in which an epitaxial layer of silicon was deposited. These results give good support to the cleanliness of the heat cleaned surfaces being considered. This conclusion is of importance as the method of U.H.V. heat cleaning must be considered to be a useful and easy to perform technique for a study of this nature.

A comprehensive data interpretation technique has been used that was considered to be the most applicable for the analysis of data from the intimate metal silicon contacts.

A theoretical model has been developed based on the original considerations of intimate metal-semiconductor contacts proposed by Heine[6] and the further developments to this concept[14]. Computations from this model have shown good agreement with the barrier heights measured for the various metal silicon contacts investigated. The values used for the electron affinity of silicon and the metal work functions being considered to be the most relevant from the reported data. The bias dependence of the surface charge due to the metal quantum tails is well demonstrated in the nature of the current-voltage characteristics of the devices. Namely the poor forward bias characteristics can be explained in terms of the variation of the potential barrier at the interface with applied bias. This effect becoming especially pronounced when considering the reverse bias characteristics of the lower work function metals investigated especially aluminium. The very soft reverse characteristics in these contacts can be attributed to the formation of a very thin potential barrier in which quantum mechanical tunnelling can become the predominant mechanism for the current transport across the interface. The temperature dependence of the experimental results have been minimal with only small departures from the expected temperature dependence from the theoretical model. These variations being mainly due to the temperature dependence of the various energy levels in the metal-silicon contacts.

Whilst there is obviously scope for future research work in this particular area it is hoped that the information obtained during this present work will contribute to a greater understanding into the true nature of the electrical behaviour at intimate metal-semiconductor interfaces.

8.3. OUTLINES FOR FUTURE RESEARCH WORK

Several points have arisen during this research work which lead to useful guides for future work both on this particular topic and also on a more diverse level. It has been well demonstrated that the nature of the silicon surface can play a dominant role in the barrier profiles obtained from the metal contacts. It would therefore be useful to obtain information with regards to interfaces involving a purer silicon substrate material if available. Float zone formed crystal silicon, which should tend to have a lower oxygen content, would be worth consideration for a further investigation. It would then be possible to provide nearer the ideal intimate metal to atomically clean silicon contact and lead to more information with respect to the effects of the metal induced surface states.

While discussing the importance of the nature of the silicon surface structure, an interesting extension to this present work would be to continue the experimental analysis by involving the use of substrates with differing surface crystal planes. At present the vast majority of investigations into the nature of metal-silicon contacts have involved the use of < 111 > orientated silicon substrate material. An investigation of this kind has been carried out using Gallium Arsenide substrate material. Smith [120] noticed a dependence of the barrier height on surface orientation. In the case of the <111> surface a value of barrier height about 0.1 eV higher than the < 100 > face was measured. The < 111 > face was intermediate between the two values. A study of contacts onto different crystal orientated substrates should yield important information with regards to the physics of the decay of the metallic quantum states into the silicon bond structure. Also one might expect the neutral level of these surface states to be at a different energy when considering differing crystal planes. However, it has been suggested by Mead and Spitzer[121] that the neutral level is purely dependent on the crystal structure and that $\emptyset_o \simeq \frac{1}{3} Eg$ may be true for all semiconductors with the diamond or zinc blende structure. Certainly data available would tend to support this view with regards germanium and various III - V compounds.

Some useful information can be derived from the data available from investigations concerning the use of chemically prepared silicon surfaces. In all the experimental work reported in the literature an interfacial layer has been present purely due to the fact that no U.H.V. cleaning procedure was undertaken prior to the deposition of the metal film. Of course the thickness of this interfacial layer is to a certain extent

arbitrary. With the predicted thickness of oxide layers involved, the theoretical analysis involving the effects of metal induced surface states can be considered to be in no way applicable. This being basically due to the interfacial layer thickness being of the same order if not greater than the expected mean penetration depth of the metallic quantum tails. Thus we can perhaps effectively consider the available data for this type of contact as representative of the original surface state analysis due to Bardeen[4] in which purely intrinsic silicon surface states are considered to be responsible for the departure from the ideal Schottky relationship. These two basic theoretical surface state models suggest that an investigation involving a control on the thickness of an interfacial oxide layer would be of great interest. This would allow data to be obtained from metal silicon contacts over a wide range of differing interfacial layer thickness. This would then lead to important information with regards to the relative effects of the metal induced surface states and the intrinsic silicon surface states and perhaps some indication into the way in which they are inter-related. This could be experimentally achieved by the leakage of controlled amounts of oxygen into the vacuum chamber immediately prior to the formation of the metal contact. A time versus oxide thickness calibration could then be achieved at a given pressure thus allowing differing controlled oxide thicknesses to be introduced to the contact. A limited investigation in this particular area has been carried out by Archer and Attala in which various silicon surfaces, prepared by cleavage under vacuum conditions, were exposed to oxygen prior to the deposition of the metal film. It is interesting to note that differing values of barrier heights were obtained from C - V measurements. This would tend to suggest that a further and more detailed study, involving U.H.V. heat cleaned surfaces, would be of merit. Greater information could now be obtained considering the more detailed data analysis techniques available in conjunction with the developing theory with regards to the true behaviour at the metal silicon interface.

At this point, it is of interest to consider the development possible in the actual techniques used for the formation of the metal-silicon interfaces as well as the various measurement techniques employed. It must be considered desirable, especially in the light of the points discussed in the previous section, to be able to carry out all the experimental procedures, including the measurement techniques, under U.H.V. conditions without the U.H.V. seal being broken throughout the whole experimental cycle. It has been pointed out that even when considering the case of intimate contacts the work function of the metal may well be different from that of the vacuum value.

Rose[122] has considered the variations that can be introduced by the different positions that the first metal atoms can occupy with respect to the semiconductor surface. In the light of the doubts that exist to the value of work function it would be useful to be able to actually measure the work function of the metal film in stitu. Doubts about the values quoted and used for the electron affinity of silicon was also discussed in the previous section. Again due to the wide range of reported values used, in metal-silicon contact analysis, it would be of importance to be able to measure this value in stitu. These various important considerations all lead to the basic advantage of such a technique in that one can reasonably neglect the possibility of any external influences or doubtful assumptions leading to misleading results being obtained. Thanalikis[34] has developed such a technique to a certain extent and has been able to perform I - V, photoelectric and C - V measurements under U.H.V. conditions after the actual formation of the metal-silicon contact. However, as already mentioned,this work involved the use of cleaved silicon surfaces which from the various points discussed in this thesis could lead to misleading results and data interpretation. However, his work has certainly indicated the practicality of a more sophisticated technique for obtaining accurately all the measurements required for a full analysis of metal-semiconductor contacts.

The use of an Auger system in the U.H.V. chamber would be desirable, as then a detailed analysis of the silicon surface would be possible at all the stages of the experimental procedure. This would then lead to more information with regards to the nature of the silicon surface used for the formation of the device. This could also be coupled to a more useful interpretation of the information available from the quadrupole mass spectrometer.

It can therefore be seen that there are several possible avenues for future research work in this field many of which have not been discussed here. Thus with more experimental data constantly becoming available on the subject of intimate metal silicon contacts, this must mean that a greater understanding can be achieved of the electronic behaviour at the interface. This will lead to more information as to the validity of considering the various theoretical approaches[6,7,8,9,10] that have been proposed on the subject of the band structure modifications at the interface. Thus with the ability to produce near the ideal intimate metal silicon interface, coupled with the capability of being able to accurately interpret the data from these interfaces, it is more likely to obtain a more concrete correlation with the predictions from a theoretical model.

In the wider aspects of the subject, the experimental procedures used with regards to the metal-silicon contacts, could be extended to an overall appraisal of metal semiconductor contacts. It has been pointed out[17,123,124] that there would appear to exist a rather fundamental transition in the electrical behaviour of metal contacts onto ionic and covalent semiconductors. It would appear that contacts involving ionic semiconductors are very dependent on the value of the metal work function, whereas co-valent semiconductors show a far lesser dependence on the variations of metal work function values. Of course many of these previous reported results must now be considered to be in some doubt in the light of this and other recent research work. However, the basic transition cannot be ignored and a study involving intimate contacts, coupled with the type of data interpretation and theoretical analysis presented during this work, could lead to a greater understanding into the wider aspects of the electrical behaviour at metal-semiconductor interfaces.

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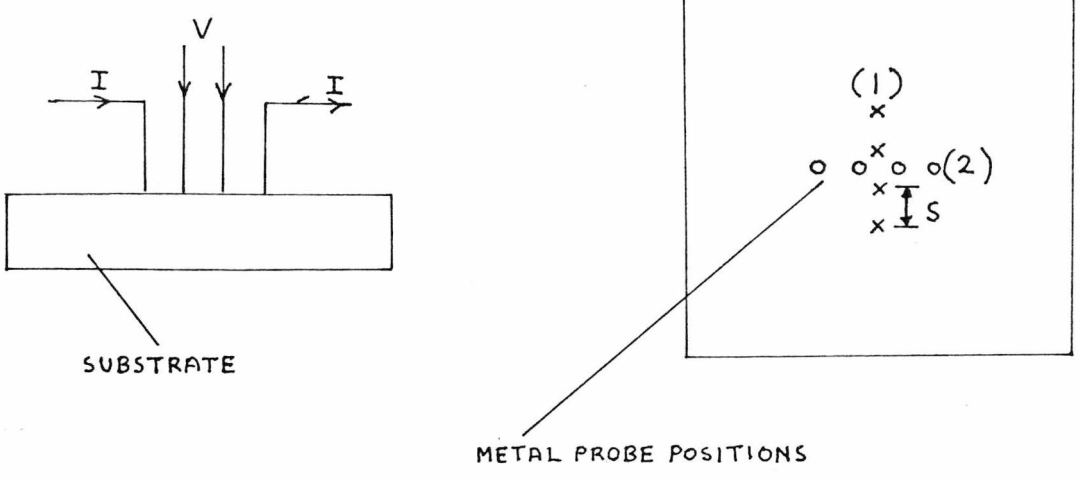
APPENDIX A

DETERMINATION OF IMPURITY CONCENTRATION

As mentioned in chapter 4 impurity concentrations were determined by employing the method of a four - point probe. Four equally spaced in-line metal probes were used to contact the silicon surface. A measured d.c. current, I, was passed through the two outside probes which induced a voltage drop, V, across the two inside probes as shown in the figure below.



The measured current and voltage were directly translated into sheet conductivity by the use of the appropriate correction factor for the substrate and probe geometry[80]. For a finite substrate size the expression becomes:

$$\frac{1}{\sigma_S} = C \frac{V}{I}$$

where C is the correction factor and σ_S is the sheet conductivity.

To improve the accuracy in determining the sheet conductivity the I - V measurements were first taken with the four probes in position (1), see figure above, and the sheet conductivity was calculated from the above equation. The measurements were then retaken with the polarity of the d.c. current reversed; and once again the sheet conductivity was evaluated. The average of these two sheet conductivities, σ_{S1}, was noted. The four-point probes were then moved to position (2), shown in the above figure, and the same procedure was adopted; this produced an average sheet conductivity, σ_{S2}. From these measurement the layer sheet conductivity was taken as

$$\left(\frac{\sigma_{S1} + \sigma_{S2}}{2}\right)$$

The impurity concentration can then be evaluated from the equation.

$$N_o = \frac{\sigma_S}{e\mu}$$

where μ is the carrier mobility.

APPENDIX B

ETCHES USED DURING THIS WORK

A GOLD ETCH

The gold etch used during this work consisted of·

200ml	deionised water
20g	potassium iodide
10g	iodine

A CHROME ETCH

The chrome etch used during this work involved the use of two mixtures, A and B, where A was:

100g	sodium hydroxide
100ml	deionised water

and B was:

400ml	dionised water
133g	potassium ferricyanide

The chrome etching was achieved by mixing 3 parts of B with 1 part of A.

A ALUMINIUM ETCH

25cc Nitric acid	5%
75cc CH_3COOH	15%
386cc H_3PO_4 Orthophosphoric acid	76%
20cc D.I. Water	4%

APPENDIX C

A SYNOPSIS OF RECENT RESEARCH WORK

In the intervening time between the conclusion of this research and the completion of this thesis it has been noted that further relevant research has been reported by various authors. It is the object of this appendix to outline these relevant topics that have been mentioned and consider them in the context of this present work. The topics can best be presented in three main areas of research.

C.1. INTIMATE METAL SEMICONDUCTOR CONTACTS

Cohen [A1] has reported calculations which give support to the model of an intimate metal-semiconductor contact proposed by Heine[6]. These calculations have shown that the prominent peak in the semiconductor band-gap arising from the existence of the dangling bond surface states is greatly reduced upon the addition of the metal to the surface. The states which appear to determine the properties of the metal-semiconductor barrier are metal induced gap states which decay into the semiconductor with a relatively short decay length. Part of the amplitude of these wave functions is concentrated in the region where the dangling bond state was prominent.

Brillson[A2] has carried out an investigation into chemical mechanisms of Schottky barrier formation. A U.H.V. study has been made of reactive and unreactive metals on a wide range of semiconductors. From a study of surface work function, band bending and chemical bonding measurements several different mechanisms of barrier formation are indicated, each determined by the degree of interface chemical reactivity. This is a similar analysis to that reported by Phillips[9,10] and used to explain the fundamental transision in electrical properties between metal contacts on covalent and ionic semiconductors[A3]. However, from the recent theoretical models[11,12,14,15] and experimental results[34] for intimate metal-silicon contacts there is no evidence to suggest that a different theoretical approach should be considered with respect to the interfaces formed during this research. However, this does give support to the value of a wider study of intimate metal-semiconductor contacts as suggested in chapter 8.

C.2. DATA INTERPRETATION AND SURFACE STATE ANALYSIS

One technique for characterising the current-voltage relationship of a metal-semiconductor contact is by the use of a pseudo thermionic emission relationship in which the true function temperature is incremented by a temperature T_o. This is often referred to as the T_o anomaly [A4]. Levine [A5] pointed out that for many metal-semiconductor contacts T_o is independent of temperature at a constant current and that T_o is actually bias dependent at a constant temperature. Levine attributed this anomaly to an exponential surface-state energy distribution. The surface state charge Q_{SS} being of the form

$$Q_{SS} = Q_C \exp\ (-\phi b/E_o)$$

Where Q_C is a constant of integration and E_o is a characteristic energy of the distribution of surface states. These surface states having a certain energy distribution fixed within the band-gap with respect to the conduction band edge in the semiconductor. Levine determined that T_o can then be given by

$$T_o = -T \left(\frac{\partial Q_{SC}}{\partial \theta}\right) / \left(\frac{\partial Q_{SS}}{\partial \phi b}\right)$$

where $\theta = \phi b - eV$, V being the applied bias and Q_{SC} is the space charge in the semiconductor. Thus from the bias variation of T_o it is possible to compute values for E_o and ϕb.

Interpretation of forward bias I - V results on this basis will lead to an ideality factor as given below.

$$n = 1 + (T_o / T)$$

The important conclusion from this work is that the dependence of barrier height on electric field at the interface can be given in the form

$$E_I \frac{d\phi b}{dE_I} = E_o/e$$

where E_I is the electric field at the interface. For the case of reverse I - V characteristics the analytic form of Levine's results [A6] can be given as

$$J_{rev} \propto E_I^{(E_o/kT)}$$

The exponential effective interface density is in fact that required to predict a linear relationship between $\ln(J_{rev})$ and $\ln(V_B)$, where V_B is the semiconductor band bending.

Jager and Kassing [A7] used this form of interpretation in an experimental investigation into the temperature dependence of I - V and C - V characteristics of Schottky barriers. It was found that the ideality factor and the barrier height were very dependent on temperature. For Al contacts onto n-type silicon the ideality factor varied from 2.5 at 20°K to 1.0 at 320°K with a corresponding variation of the measured barrier height from < 0.3 eV to > 0.6eV. These results could be fitted to an expression for the ideality factor of the form

$$n = a + T_o/T$$

A value of a different from unity being necessary.

One of the most interesting outcomes of this work was the fact that the results were found to be independent of the pressure at which the contact was formed. Pressure ranges from $\leq 10^{-5}$ torr to $< 10^{-8}$ being considered. This would certainly not be expected in the light of all the discussion on this topic in this present thesis.

Crowell[A8] has investigated the physical significance of the T_o anomaly. Comparisons are drawn between the Levine model [A5, A6] of an exponential energy density of interface states to explain the To anomaly and with the Bardeen interface model[4] with a parabolic density of surface states. Crowell observed that except for cases in which the characteristic energy E_o is less than kT, the two models were in good agreement but with the Bardeen model being more physically representative. However, difficulties are encountered in these models when E_o is less than kT.

The surface state analysis reported by Cowley and Sze[5] has been extended by Wu[A9] by considering the effects of a surface fixed charge and the voltage drop across the interfacial layer under non equilibrium conditions. The result of this positive surface fixed charge is to reduce the barrier height and to cause higher reverse currents than expected. The voltage drop across the interfacial layer will lead to an increase in the ideality factor and the voltage dependence of the reverse current. This being attributed to a lower effective barrier height for the reverse bias case. Wu suggests that the interfacial states

are dependent on the orientation of the surface and this can explain surface orientation dependence on the measured values of barrier heights in certain cases. It is interesting to note that there are certain similarities in Wu's conclusions and the results predicted by the theoretical model presented in this thesis.

Howes, Morgan and Al-Baidhawi[A10] have reported a numeric optimisation technique in order to study the effects of surface states on the I-V and C-V characteristics of metal-semiconductor contacts. Their theoretical model is based on the same approach used in this thesis, namely the effects of the metal quantum tails decaying into the semiconductor band-gap. The surface states are assumed to exist over the energy range between the metal Fermi energy and the valence band in the semiconductor, and that they are uniformly distributed over this energy range. This type of distribution of surface states is however in disagreement with the theoretical model proposed in this thesis and by other authors[6,15]. The same form of exponential decay of the metal quantum states into the band-gap of the semiconductor is used. The fitting of the experimental data to the theoretical model is achieved by the determination of an error function between the experimental I-V and C-V results and the theoretical values. The minimisation being achieved by the use of a quasi-Newton method, which requires first derivatives of the function with respect to its various parameters. By the use of this technique it was possible to obtain good agreement between the C-V and I-V characteristics with respect to the surface state parameters. Direct comparison between this work and the research work reported in this thesis is not possible due to the lack of detailed experimental information on the formation of the devices and also the differences in the surface state parameters used in the theoretical models.

C.3. OTHER RELEVANT RESEARCH WORK

Further to the ageing process reported by Turner and Rhoderick[16] involving contacts where an interfacial layer of oxide is present. Ponpon and Siffert[A11] have observed ageing effects on metal-silicon contacts which have been formed by chemical cleaning of the silicon surface and deposition of the metal contact at a pressure of $\leq 10^{-5}$ torr. A close relationship has been found between this ageing process and the value for the heat of formation of the oxide of the

particular metal involved. This is observed in a fundamental difference in the extent of the ageing process in contacts involving metals such as gold and silver compared with aluminium.

A study into the controlled formation of an interfacial oxide layer, as suggested in chapter 8, has been performed by Mottram, Northrop, Read and Thanailakis[A12]. Initially atomically clean silicon surfaces were produced under U.H.V. conditions by both cleavage and by heat cleaning. These surfaces were then deliberatly contaminated with oxygen in a controlled manner. During this contamination the work function changes were studied using the Kelvin vibrating capacitor technique. The metal contact was then formed by the evaporation of copper or gold onto the surface without breaking the vacuum. The barrier heights of the various contacts were then determined by the use of C-V and I-V measurements as well as photoelectric methods. In general the barrier heights obtained from C-V measurements were greater than those determined from the other two techniques. This result being in accordance with the expected barrier profile at the interface as discussed in chapter 7. However the most significant observation was that this difference was found to decrease with increasing oxygen exposure. This is certainly an interesting observation as this result may be attributed to the differing effects of the surface states on the barrier profile at the interface as the interfacial layer of oxygen is increased. Hence with less band bending at the interface the I-V results for barrier heights will tend towards those obtained from C-V measurments. It may also be the case that differences are being observed between the effects of the metal quantum tails and the intrinsic silicon surface states. However, with the many effects involved,care must be taken in order to obtain a useful interpretation. Also observed was an ageing process on contacts involving copper, perhaps supporting the results reported by Ponpon and Siffert[A11].

Finally, interest has been shown recently into techniques available for controlling the barrier height of metal-semiconductor contacts. The barrier height is a critical parameter for a Schottky contact to be successfully used in various microwave and integrated circuit applications. It has been shown that the presence of a surface layer having a conductivity type opposite to that of the bulk semiconductor, results in an increase of barrier height which can be suitably controlled by varying the doping concentration[A13,A14]. Recent

theoretical analyses [A15,A16] have indicated that the degradation to the rectification properties caused by this interfacial layer can be minimised by careful control of the doping concentration and keeping the thickness to a minimum.

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