

FIGURE 6.2 Modified N.E.C. Response Registers Board 13

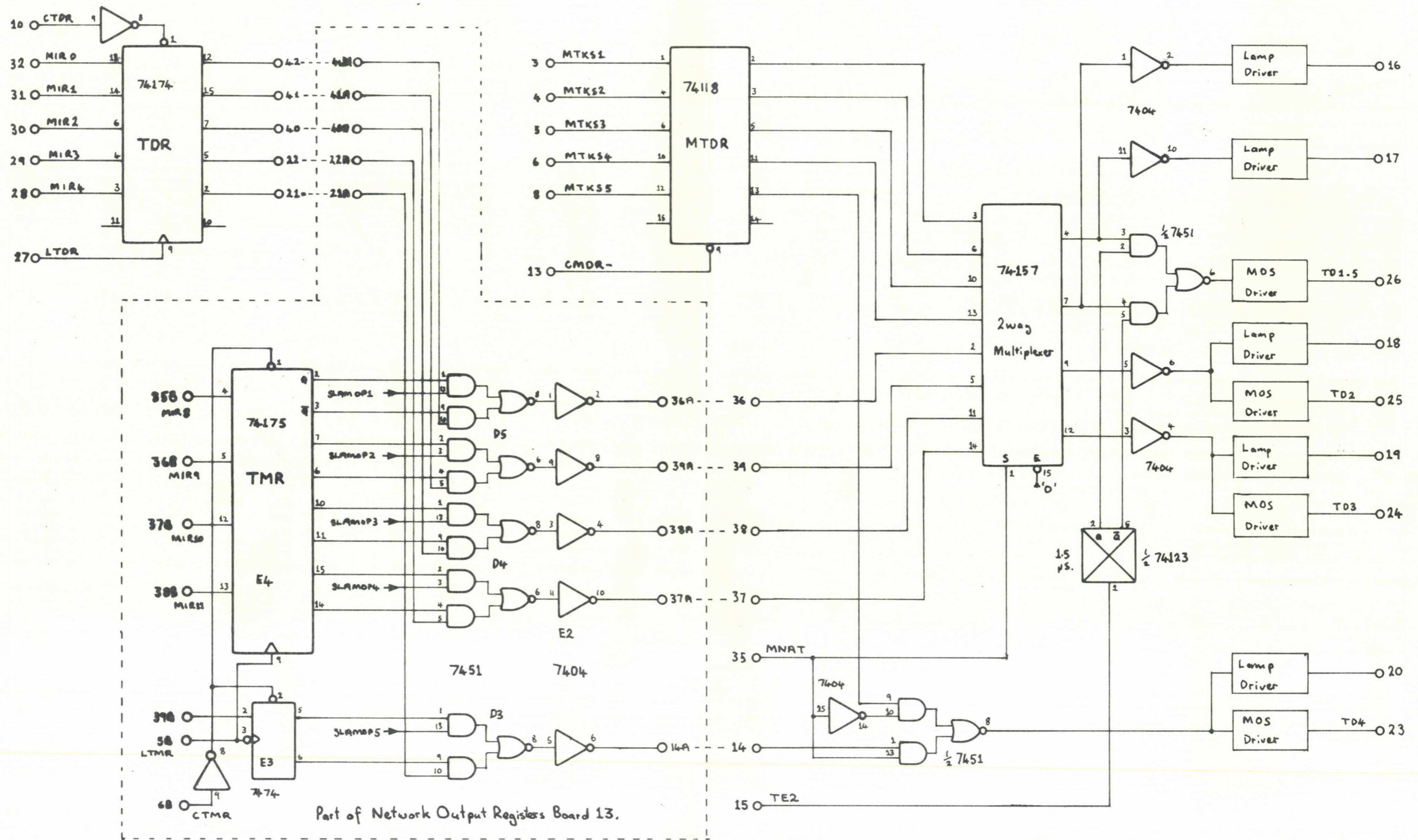


FIGURE 6.3 Teach and Teach Mask Register Logic Board 12

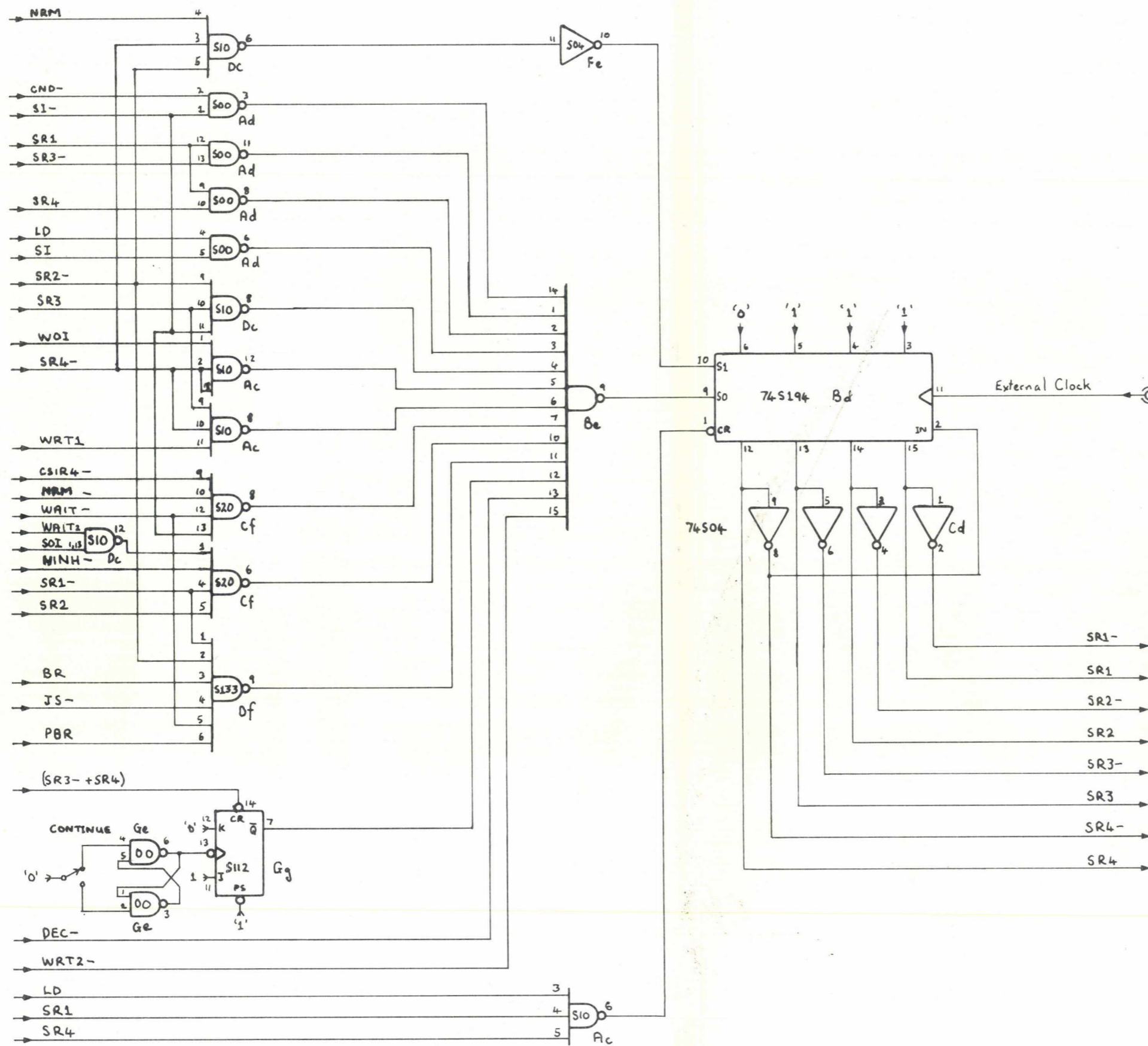


FIGURE 6.19 Clock Generator (C-module)

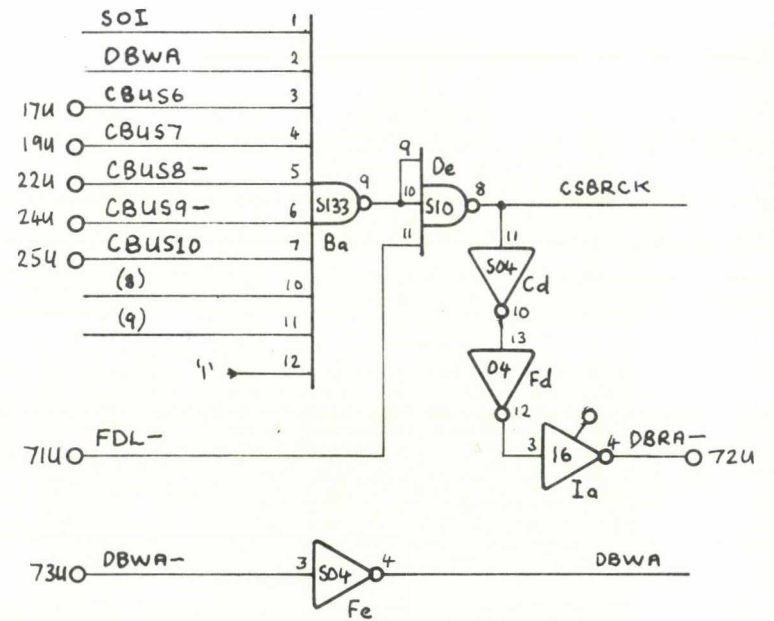
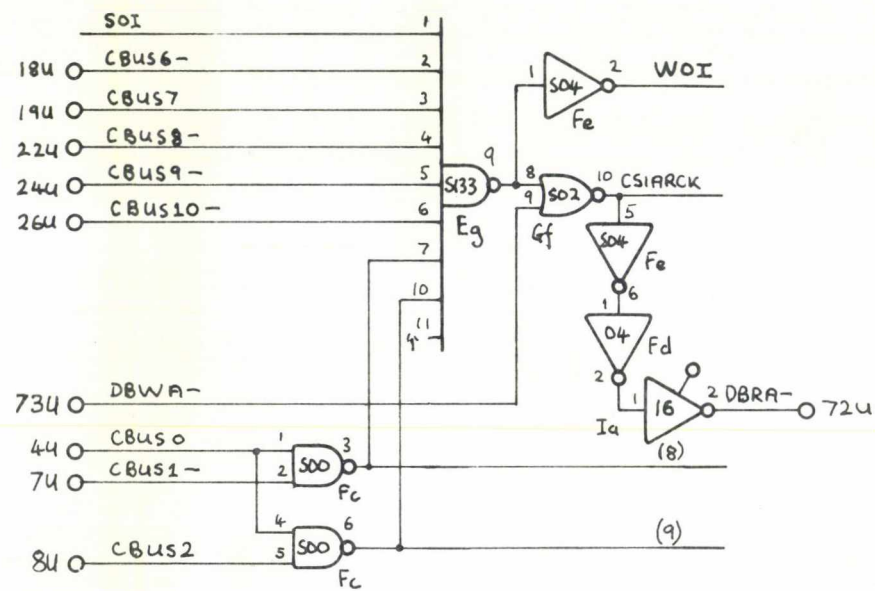
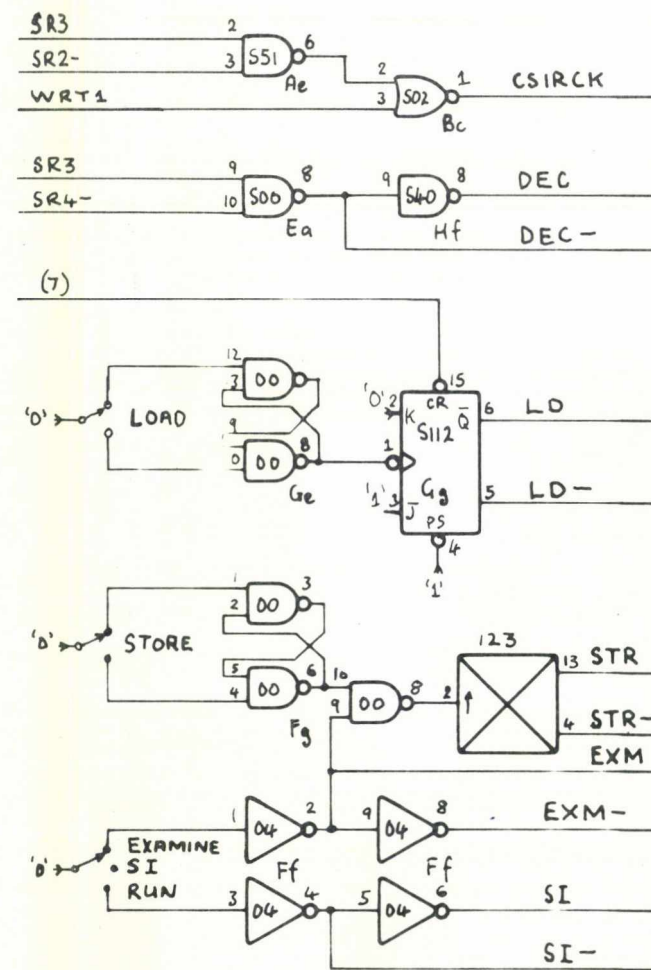
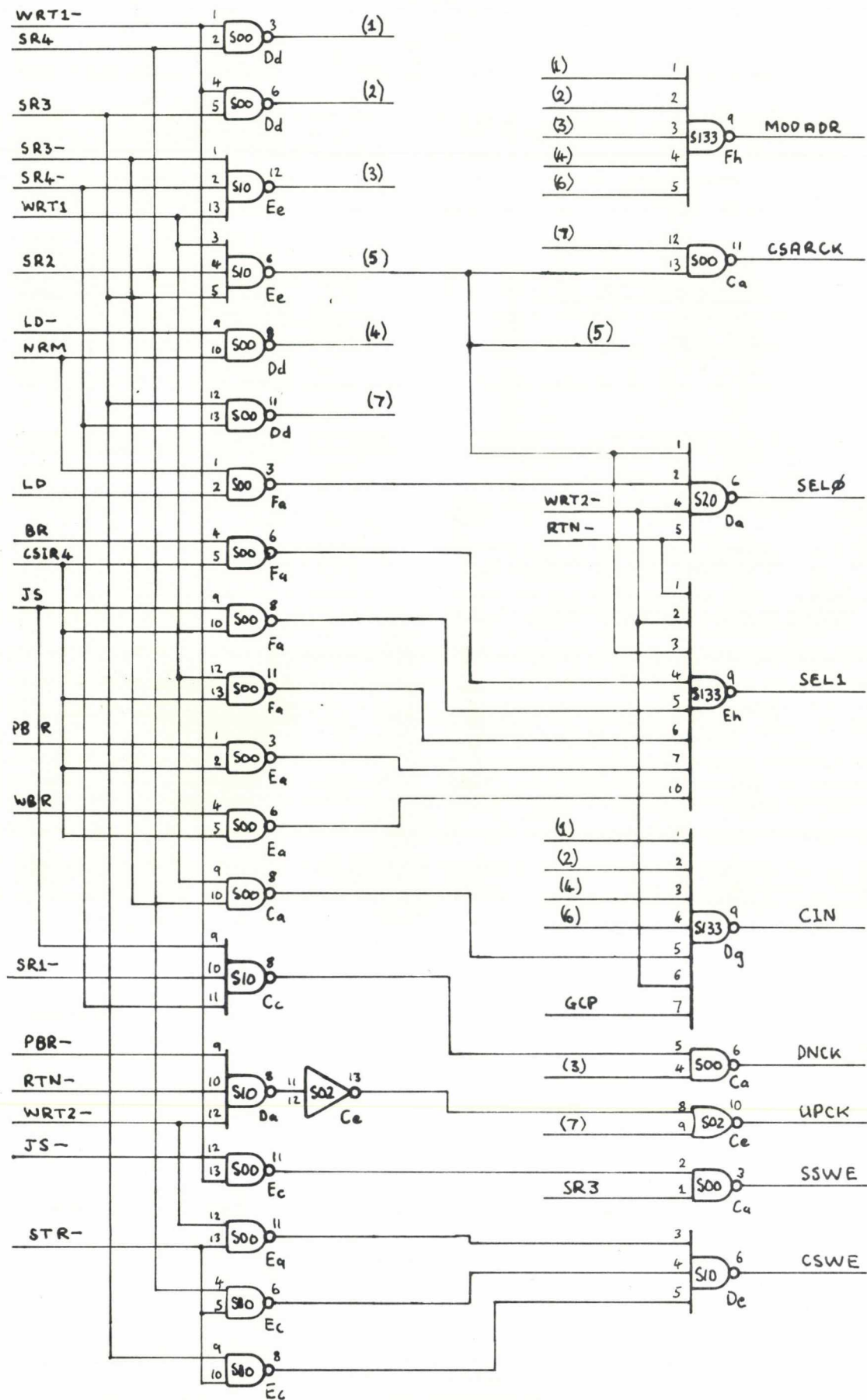


FIGURE 6.20 Control-Order Logic

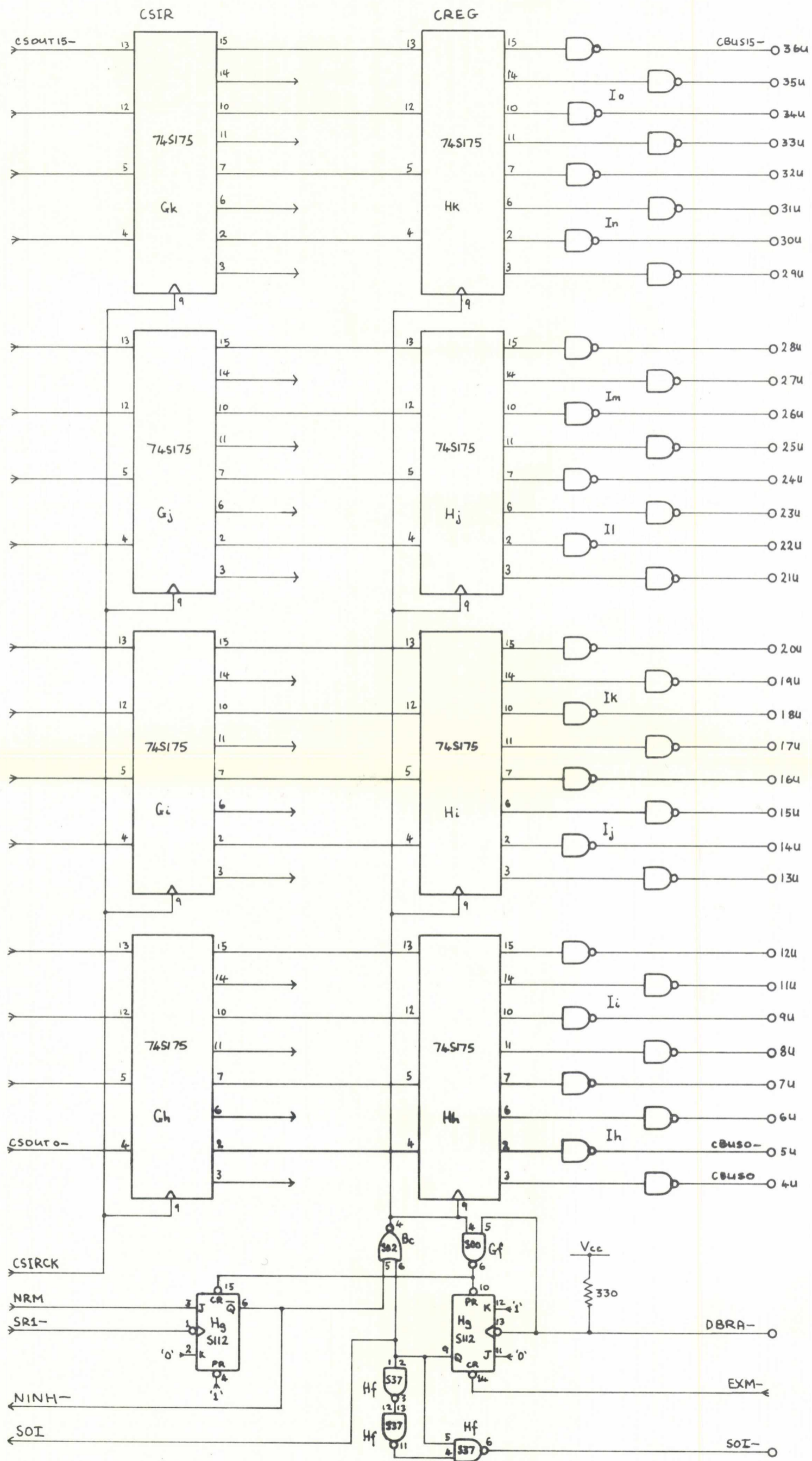


FIGURE 6.21 Micro-Instruction Pipeline

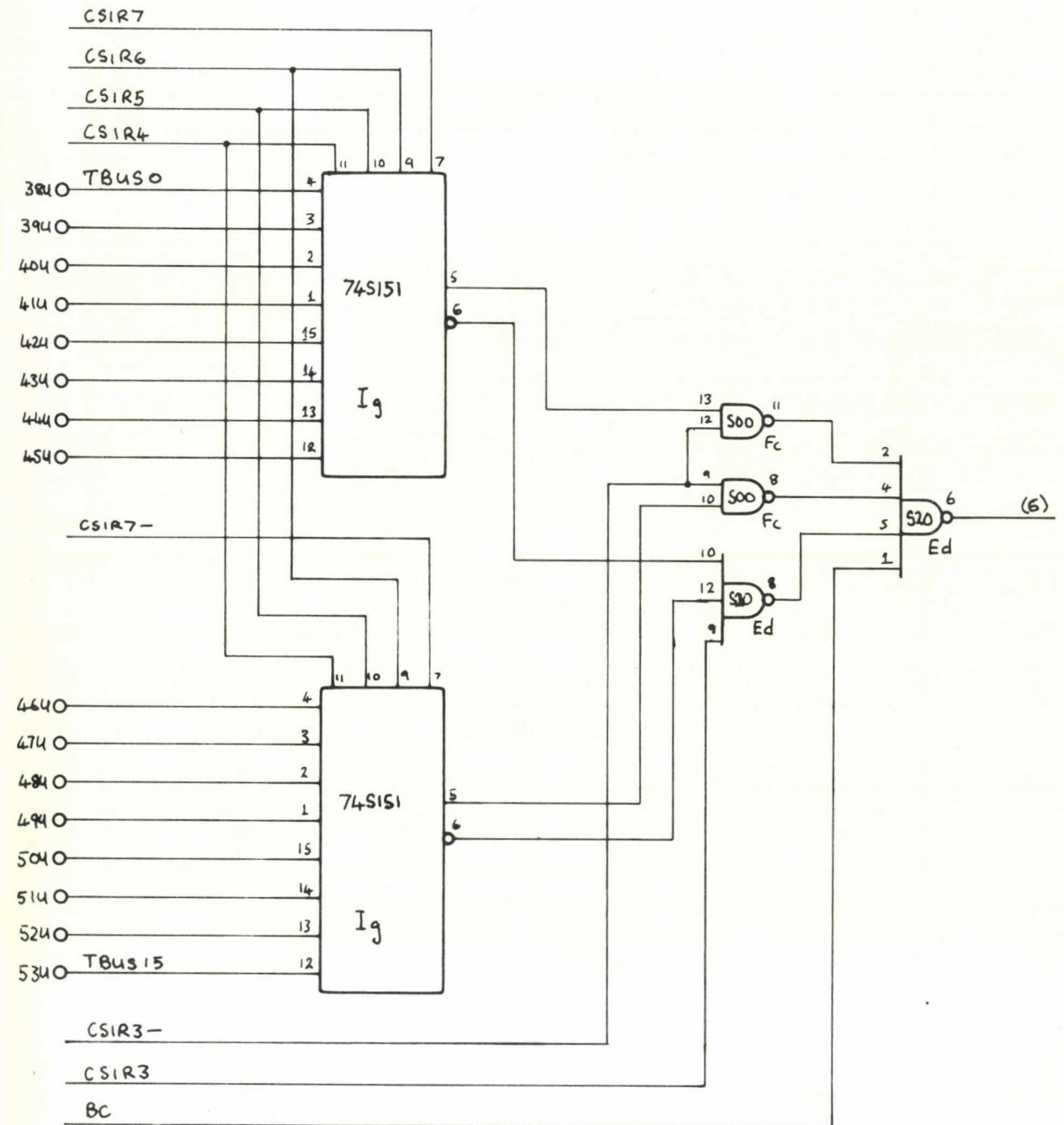
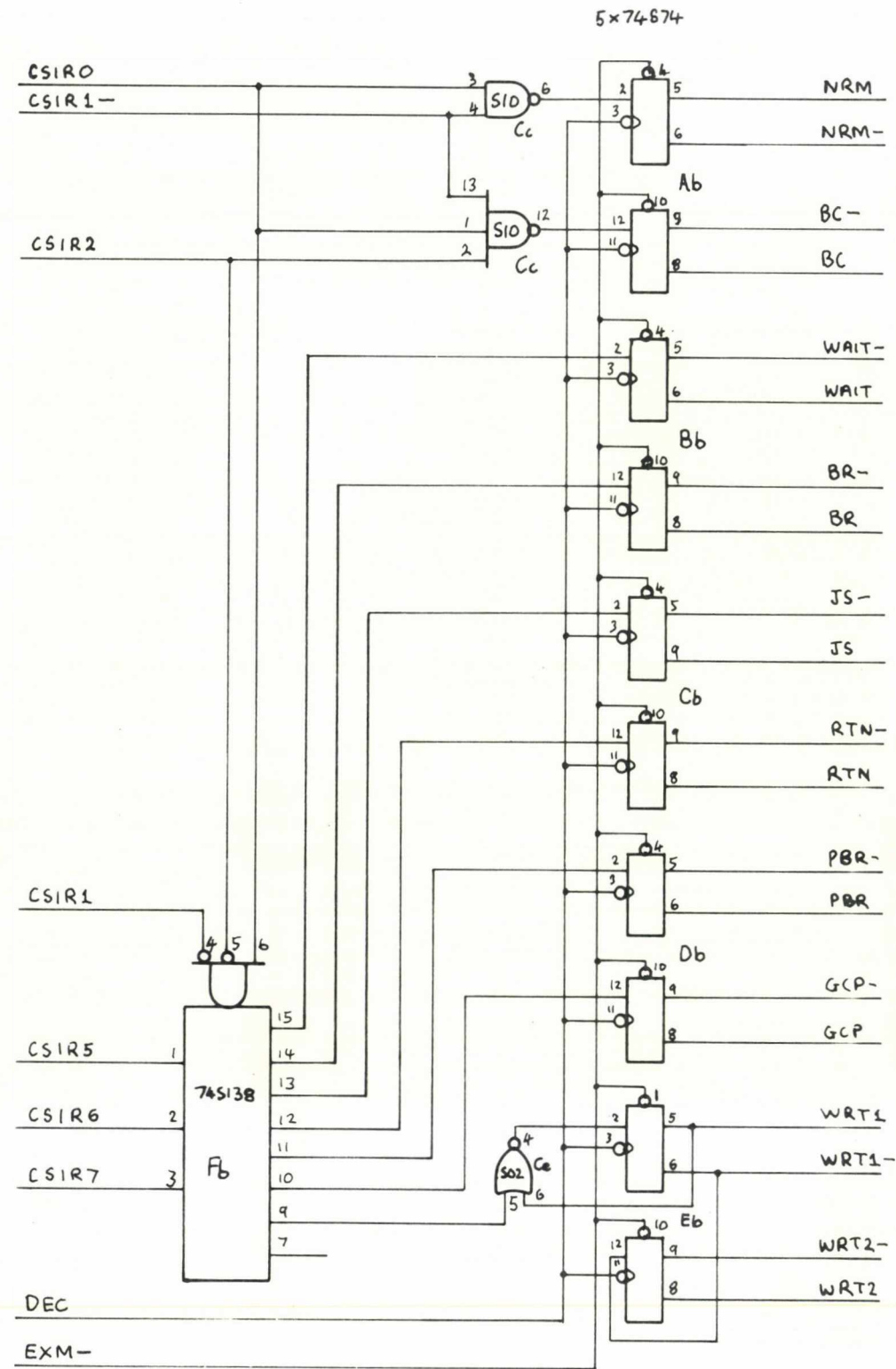
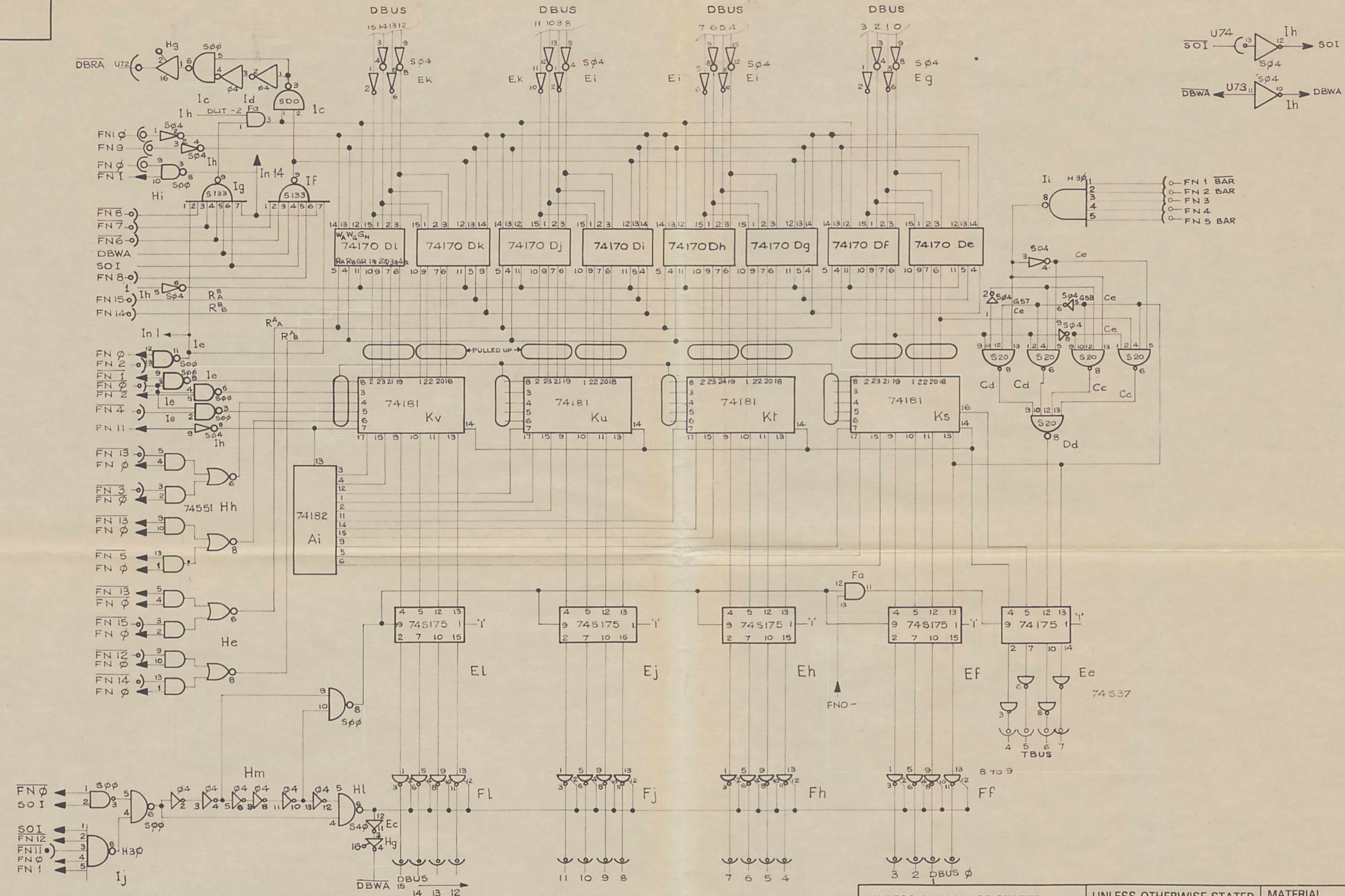


FIGURE 6.22 Micro-Instruction Decode



UNLESS OTHERWISE STATED ALL DIMENSIONS ARE IN MILLIMETRES.	UNLESS OTHERWISE STATED TOLERANCES ± 0.3 M/C SURFACE 3.2 / μ C.L.A. FINISH ✓ ALL SHARP EDGES REMOVED MAX. 0.3 RAD. OR CHAMFER	MATERIAL	DRAWN	DATE
		FINISH	APPROVED	DATE
SCALE				

TITLE MINERVA MODULAR MAPPING PROCESSOR :-
ARITHMETIC LOGIC UNIT, ACCUMULATORS MODULE

FIGURE 6.23

ISSUE No.	ALTERATION	DATE

BRUNEL UNIVERSITY	KINGSTON LANE UXBRIDGE MIDD.	DRG. No. MMP 4
	SCHOOL OF:- ENGINEERING	

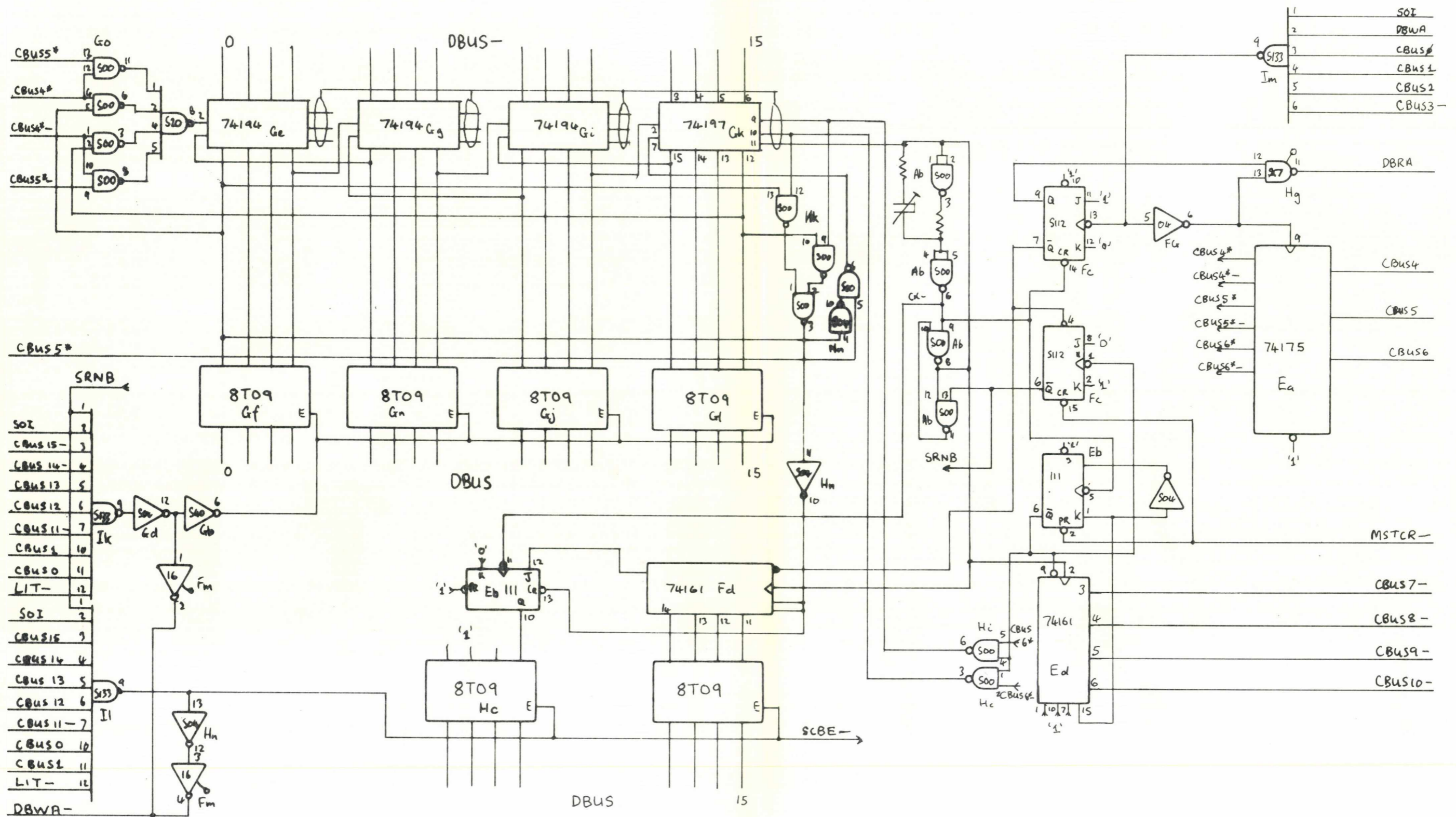


FIGURE 6.24 Shifter & Bit Counter Module

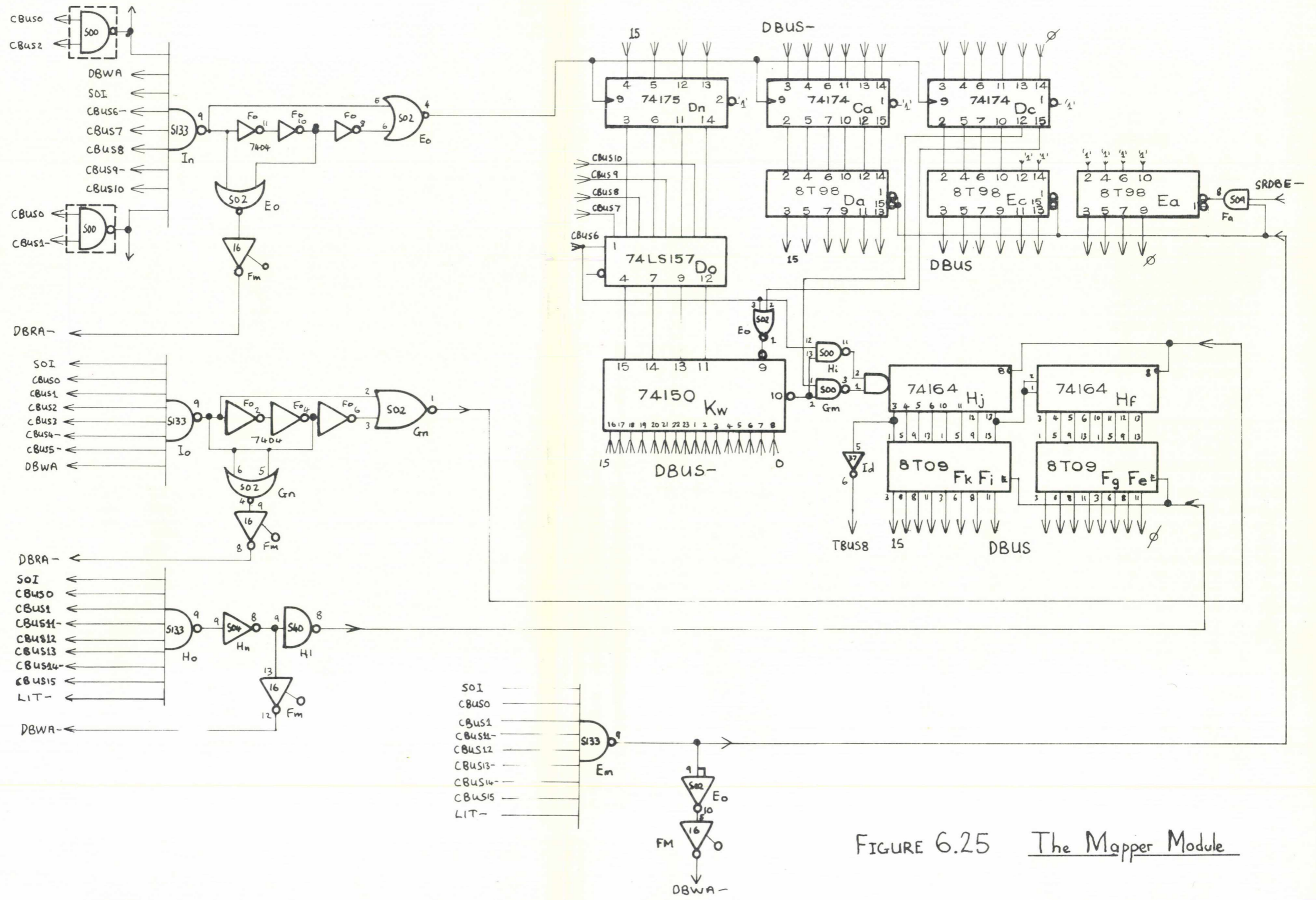


FIGURE 6.25 The Mapper Module

BRUNEL UNIVERSITY		KINGSTON LANE UXBRIDGE MIDD.	SCALE
SCHOOL OF ENGINEERING		DEPT. OF ELECTRICAL ENG.	DRG. No.
TITLE			

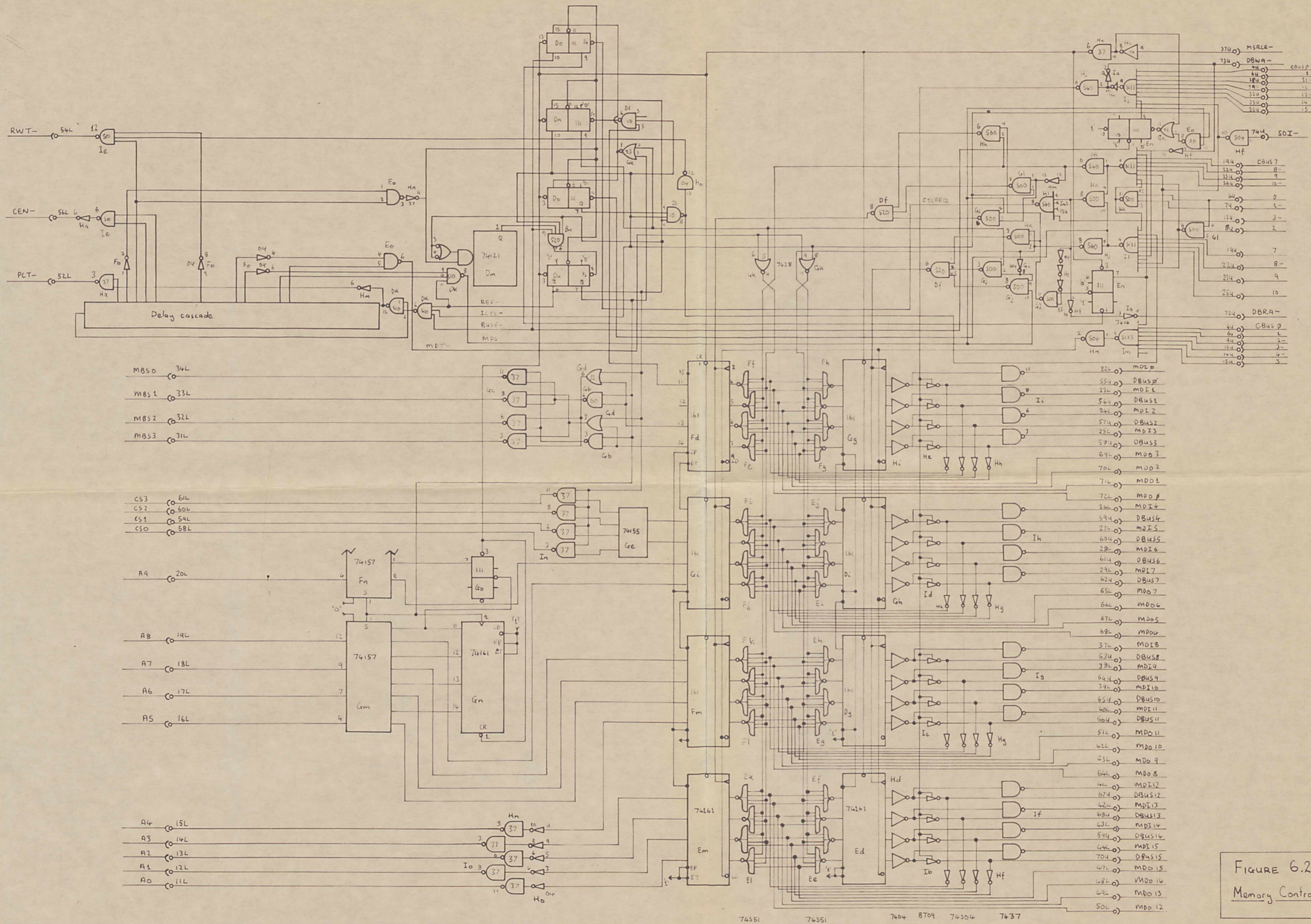


FIGURE 6.27
Memory Controller Logic

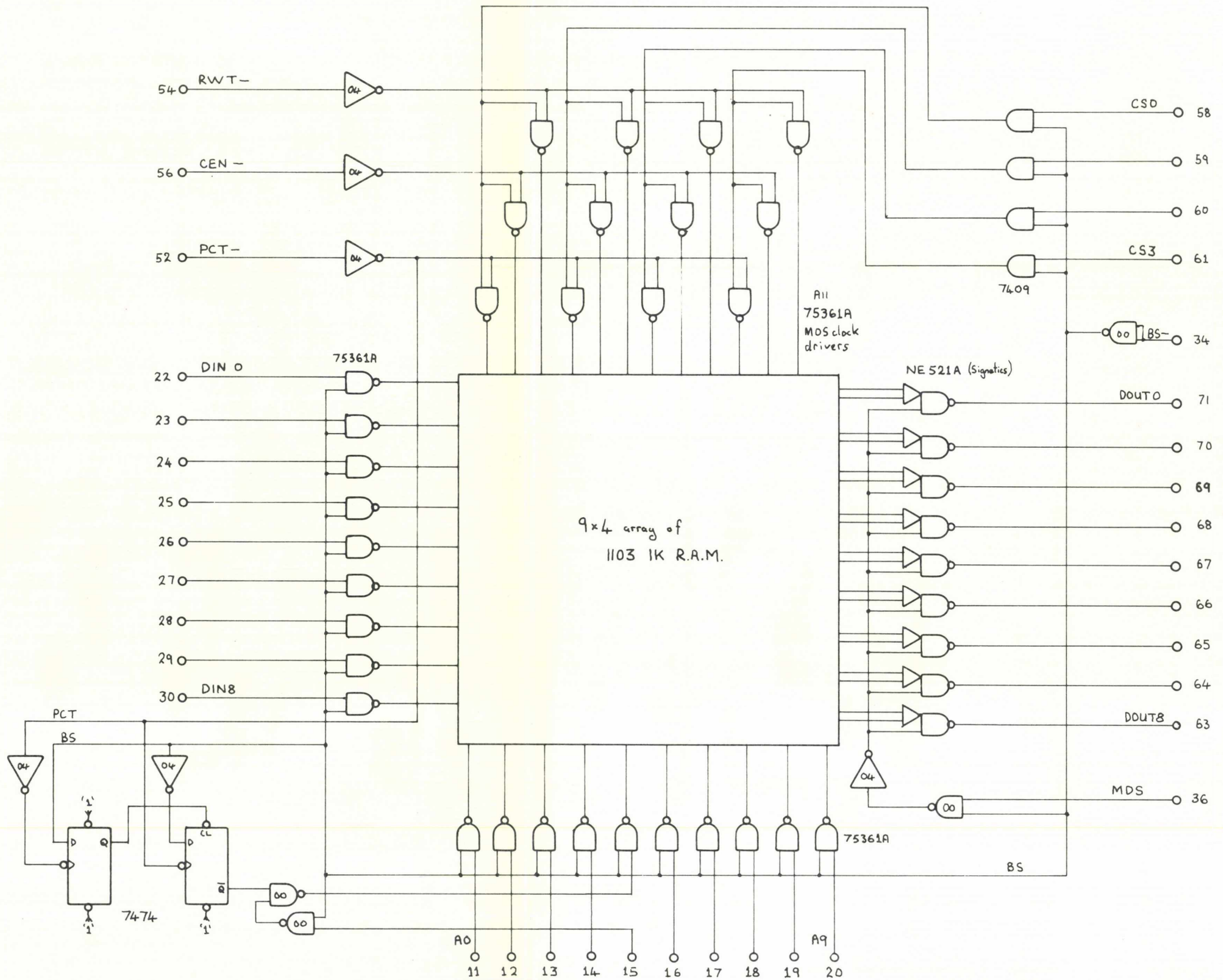
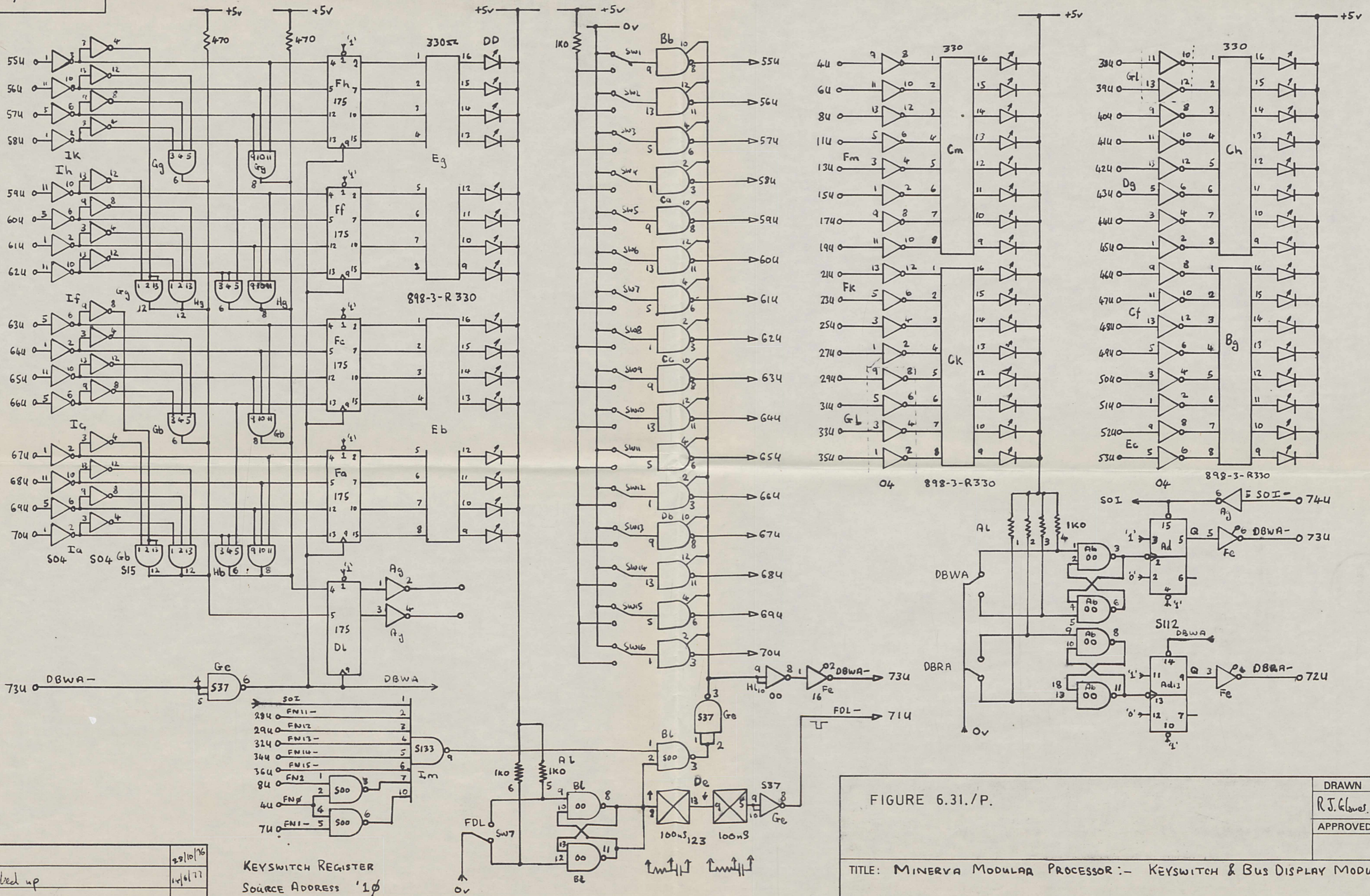


FIGURE 6.28 M.O.S. Memory Board

DBUS DISPLAY

FNBUS DISPLAY

TBUS DISPLAY



1		29/10/76
2	marked up	14/6/77
ISSUE No.	ALTERATION	DATE

KEYSWITCH REGISTER
SOURCE ADDRESS '10'

FOR EXPLANATION OF DIMENSIONS, NOTES ETC., SEE BS 308.

FIGURE 6.31./P.

TITLE: MINERVA MODULAR PROCESSOR :- KEYSWITCH & BUS DISPLAY MODULE.

BRUNEL UNIVERSITY

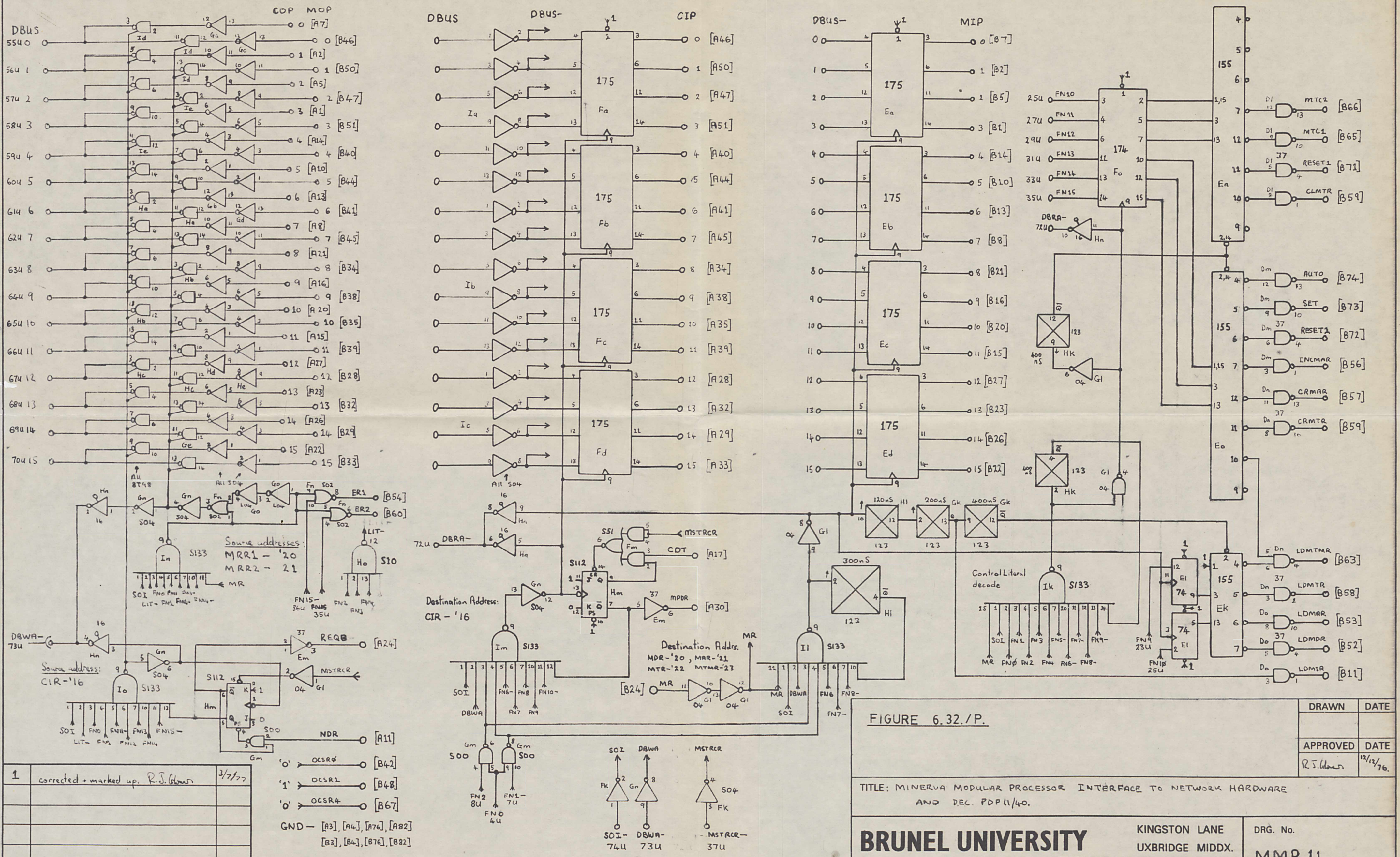
KINGSTON LANE
UXBRIDGE MIDDX.
TEL 37182 EXT 308

DRG. No.
MMP/10

SCHOOL OF: ENGINEERING

DEPT. OF: ELECTRICAL ENGR.
& Electronics.

DRAWN	DATE
R.J. Glover	26/10/76
APPROVED	DATE



1	corrected + marked up. R.S. Ghorar	3/7/77
ISSUE No.	ALTERATION	DATE

- '0' → OCSR0 [B42]
- '1' → OCSR1 [B48]
- '0' → OCSR4 [B67]
- GND - [A3], [A4], [A76], [A82]
- [B2], [B4], [B76], [B82]

Key: [Bn] - MINERVA Interface connector ; [An] - Computer interface connector.

FIGURE 6.32./P.

DRAWN	DATE
APPROVED	DATE
R.S. Ghorar	12/12/76

TITLE: MINERVA MODULAR PROCESSOR INTERFACE TO NETWORK HARDWARE AND DEC. PDP11/40.

BRUNEL UNIVERSITY

KINGSTON LANE
UXBRIDGE MIDDX.

DRG. No.
MMP 11.

SCHOOL OF: ENGINEERING

DEPT. OF: Electrical Engineering and Electronics.