Solution processed InAs nanowire transistors as microwave switches

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Abstract

We demonstrate the feasibility of using self-assembled InAs nanowire bottom-gated field-effect transistors as radio-frequency and microwave switches by direct integration into a transmission line. This proof of concept is demonstrated as coplanar waveguide (CPW) microwave transmission line, where the nanowires function as a tunable impedance in the CPW through gate biasing. The key to this switching capability is the high-performance, low impedance InAs nanowire transistor behavior with field-effect mobility of ~300 cm^2/Vs, on/off ratio of 10^3 and resistance modulation from only 50 Ω in the full accumulation mode, to ~50 kΩ when the nanowires are depleted of charge carriers. The gate biasing of the nanowires within the CPW, results in a switching behavior, exhibited by a ~10 dB change in the transmission coefficient, S_{21}, between the on/off switching states, over 5-33 GHz. This frequency range covers both the

microwave and millimeter-wave bands dedicated to IoT and 5G applications. Demonstration of these switches creates opportunities for new class of devices for microwave applications based on solution processed semiconducting nanowires.

1. Introduction

Printed electronics offers significant advantages over conventional processing for radio-frequency (RF), microwave, and mm-wave applications, enabling rapid maskless prototyping, low temperature processing, and high density integration of microwave elements on large-area, light-weight flexible substrates.[1] Printable filters,[2] antennas,[3] true-time delay lines,[4] wearable frequency selective surfaces (FSSs),[5,6] reconfigurable antennas,[7] phase-arrays,[8] and reflect arrays[9] have been realised, which can enable wireless sensors in internet of things (IoT)[10] and high data rate mm-wave fifth generation (5G) communications.[11,12] Microwave switches are key to enable reconfigurable antennas, arrays and FSSs, to modify their radiation pattern, resonant frequency, and polarization.[13,14]

Solution processable nanomaterials permit the integration of semiconductors and conductors, using low-temperature and inexpensive processing capability while compatible with flexible substrates. Main classes of solution processable semiconducting materials are conjugated molecules, carbon nanotubes (CNTs), graphene flakes (GFs), and inorganic semiconducting nanoparticle inks, including semiconducting nanowires (NWs). Although organic semiconductors are the most convenient for solution based deposition, the low charge carrier mobility, 0.1 - 10 $cm^2V^{-1}s^{-1}$ [15][16] of organic printed FETs results in very high device resistance from tens of kΩ to MΩ, limiting their application in microwave circuits. Other materials, such as CNTs and GFs, require chemical functionalization to be solution processable, which degrades charge transport properties resulting in field-effect mobilities of 9 - 42 $cm^2V^{-1}s^{-1}$ for CNTs [17–19] and below 1.2 $cm^2V^{-1}s^{-1}$ for GFs.[20–22] These low mobilities give rise to high

channel resistances, thus making these materials less desirable for solution processable high performance microwave switches. The most promising class of materials are semiconducting single crystal NWs, such as III-V materials, that possess high charge carrier mobility in the range of hundreds to few thousand $cm^2V^{-1}s^{-1}$,[23,24] and they do not require surface functionalization for ink formulations.

In this work, we focus on solution processable InAs NWs due to the high electron mobility, reaching 6500 $cm^2V^{-1}s^{-1}$ at room temperature,[25] and low contact resistance with metal tracks,[26–28] thereby avoiding the very resistive Schottky barriers common with other semiconducting NWs.[29] Additionally, InAs has high electron affinity of 4.9 eV[30] and Fermi level pinning near the minimum of the conduction band,[31,32] which helps to fabricate devices with excellent Ohmic contacts. However, Fermi level pinning can cause surface states impacting the on/off ratio and sub-threshold swing in FET devices.[30] Regardless of the issues caused by the surface states, common for all semiconducting NWs, InAs nanowires have been shown to be excellent candidates for high frequency FETs, in amplifier configuration, as they have reached a cut-off frequency of 103 GHz and maximum oscillation frequency of 155 GHz.[33]

2. InAs NW FET coplanar waveguide switch

2.1. The concept of the switch

This paper presents a solution processed coplanar waveguide microwave switch, based on high performance InAs nanowires operating from 5 to 33 GHz. Switching is accomplished by driving ~1000 InAs nanowires between depletion high resistance state (>50 kΩ), when the nanowires are practically imperceptible to the microwaves, and the accumulation low resistance state (~50 Ω), where there is significant absorption of the microwave signal by the nanowires, resulting in ~10 dB signal transmission variation between the ‘on’ and ‘off’ states.

A coplanar waveguide (CPW) was chosen as basis for the nanowire-based microwave switch as the frequency response of CPW with parasitic capacitances associated with field-effect transistor device structure is superior to that of microstrip design. The CPW has a center conductor and two outer grounded conductors that all support travelling electromagnetic (EM) waves (see Figure 1a).

2.2. InAs nanowire switch

To create the nanowire-based switch, it is important to have a very low channel resistance in the 'on' state, and correct switch dimensions to provide close to 50-Ω characteristic impedance. Very low channel resistance, coupled with high on/off current ratio is a significant challenge for solution processed nanowire FETs, and it has been addressed in the device design described below.

The gaps in the CPW device were bridged with single crystalline InAs NWs, built on top of a doped Si wafer with 1.5 μm thick silicon oxide (SiO_2) layer, as illustrated in Figure 1a. The Si/SiO_2 wafer provides a convenient substrate for the initial demonstration of the NW FET microwave switch as the fabrication processes on Si/SiO_2 are well developed for nanowires, and the doped Si acts as a common gate for the nanowire-based FET device. To achieve a low FET channel resistance, the gaps between the center conductor and grounds were designed to be 2.5 μm. The signal line and ground line widths are 6 and 20 μm wide respectively. To accommodate conventional microwave ground-signal-ground measurement probes with 150 μm spacing, tapered lines were designed to connect to the CPW as shown in Figure 1b. The section between the dashed lines, included in Figure 1b, indicates the 500 μm long nanowire FET region of the switch. The dashed lines also indicate the references planes for the S-parameter measurements. Figure 1c shows an SEM image of the self-assembled NWs in the CPW, where the nanowires were deposited from dispersions in anisole, using an electric-field assisted dielectrophoresis (DEP) process.[23,34] The total number of NWs in the device is

estimated to be ~1000 and though their distribution is not homogeneous, the length of the CPW (l= 500 μm) is much smaller than the wavelength (λ≈ 11.5 mm) of the microwave signal (at 26 GHz), so should not affect the device performance. A scanning-electron-microscopy (SEM) image is presented in Figure 1c, showing the 50 nm diameter InAs NWs bridging the gaps of the CPW.

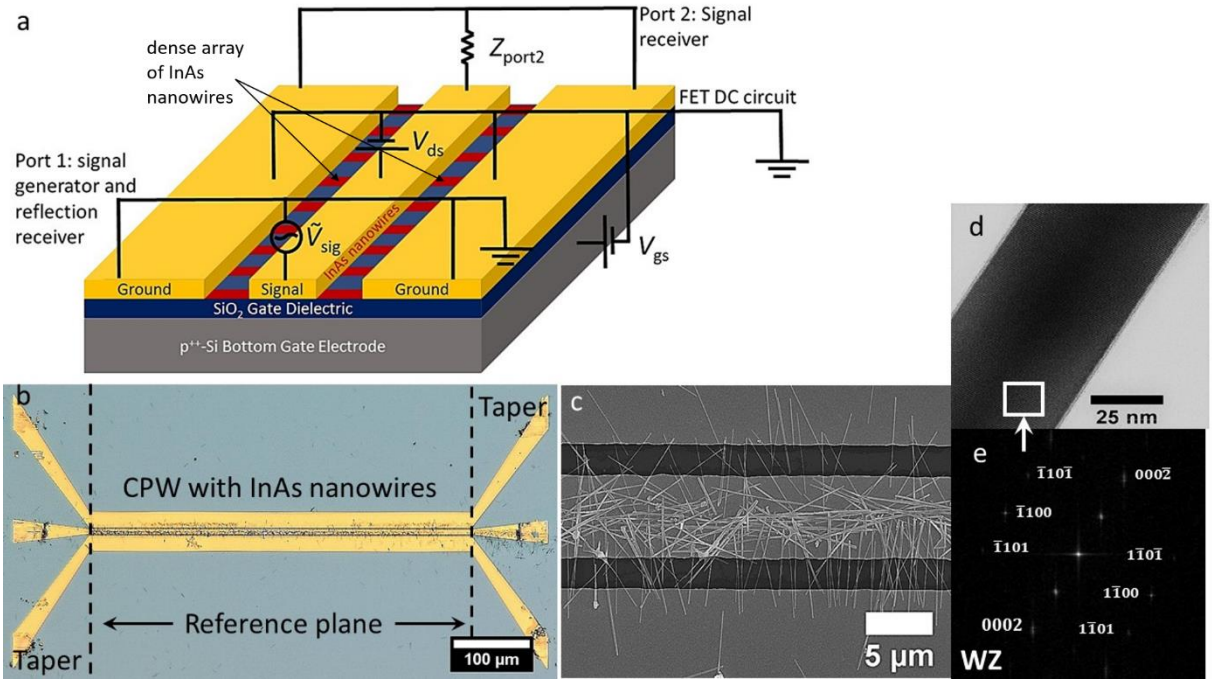

Figure 1. ***a)*** *An illustration of the nanowire-based switch, showing the coplanar waveguide with central signal line and two ground lines bridged by nanowires. By applying a DC gate voltage (Vgs) to the common-gate p^{++}-Si substrate, the nanowire transistor channel is driven between accumulation, low resistance state (positive V_{gs}), and depletion, high resistance (negative V_{gs}) state. Biasing circuit connections used to conduct full FET DC characterization are shown in the middle, with ground lines of CPW serving as FET source contacts, and the conductor line serving as FET drain contact. RF characterization was conducted at different DC bias voltages applied to the gate, and two microwave ground-signal-ground probes were connected to port 1 and port 2 respectively. Reflected and transmitted signals were measured at port 1 and port 2 using vector network analyzer, when the gate voltage drives the FET between depletion and accumulation.* ***b)*** *Optical microscope image of the CPW switch with InAs NWs assembled in the gaps of the CPW and the tapered lines. The width of the signal and ground lines are 6 μm and 20 μm respectively. The length of the CPW forming the switch is 500 μm, as indicated between the dashed lines. Tapers at the ends of the CPW were made for the microwave probes.* ***c)*** *SEM image of InAs NWs in the 2.5 um CPW gaps.* ***d)*** *STEM image of the InAs NW in the middle of the NW.* ***e)*** *indexed FFT of the corresponding areas marked areas in (d).*

The diameter and crystal structure of the InAs NWs were investigated using scanning transmission electron microscopy (STEM) analysis (Figure 1d) and the corresponding fast Fourier transformations (FFTs) (Figure 1e). As reported previously,[35] the length of the InAs NWs have fault-free stacking WZ structures, except for the seeded tip, which exhibits a zinc blend (ZB) due to post-growth cooling. The diameter of the InAs NWs was 50 nm with a native oxide layer <5 nm. More detailed TEM analysis is presented in Supporting Information. The specific fabrication steps of nanowire-based switch devices are provided in Experimental Section.

For high-frequency characterization of the switches, 2-port scattering parameters (S-parameters) were measured using a vector network analyzer (VNA) (Experimental Section). The S-parameters represent the ratio of the incident to outgoing waves at the ports of the device. The reflection coefficient of port 1 is denoted by S_{11} and the transmission coefficient from port 1 towards port 2 is denoted by S_{21}.

Under zero or negative gate bias conditions, the conductance of the nanowires is very low and the NWs have minimal effect in the CPW transmission line performance, resulting in a low S_{11} and a high S_{21}. In this paper these conditions will be referred to as “FET is OFF” and “closed state” of the switch.

Under a positive and increasing gate bias, the conductance of the NWs increases, and their resistance is reduced. This results in a decreasing impedance between the signal and ground lines of the CPW line, resulting in an increase in the reflection and a decrease in the transmission coefficients of the switch. This condition will be referred to as “FET is ON” and “open state” of the switch.

2.3. InAs NW FETs DC performance

To evaluate initial DC performance of the InAs NW-based switch, transistor characterization was performed using an Agilent 2902B analyzer under a dry nitrogen purge, at the same gate biasing voltages, as used for gate bias in microwave characterization (V_{gs} from -60 to 100 V). Considering this FET as classical MOSFET operating in the linear regime,[36] the field-effect mobility μ_{eff} can be calculated as: [37]

$$\mu_{\mathrm{eff}} = g_{\mathrm{m}} \frac{1}{V_{\mathrm{sd}}} \frac{L_{ch}^2}{C_{\mathrm{ox}}} \quad (1)$$

where μ_{eff}, g_m, C_{ox}, V_{sd} and L_{ch} are field-effect mobility, transconductance $g_m = (\frac{\partial I_{sd}}{\partial V_{sg}})|_{V_{sd}}$, gate capacitance, source-drain voltage and transistor channel length, respectively. Calculation of the C_{ox} requires cylinder-on-plate model expression given by: [38]

$$C_{\mathrm{ox}} = N \frac{2\pi\varepsilon_0\varepsilon_{\mathrm{r,eff}} L_{\mathrm{ch}}}{\cosh^{-1}\left(\frac{R_{\mathrm{NW}}+t_{\mathrm{ox}}}{R_{\mathrm{NW}}}\right)} \quad (2)$$

where ε_0=8.85·10^{-12} F m^{-1}, $\varepsilon_{r,eff}$, R_{NW}=25 nm, N~1000 *a*nd t_{ox}=1.5µm are vacuum permittivity, effective dielectric constant of SiO_2 and air, radius of NW, number of NWs in the channel and oxide thickness, respectively. For nanowires positioned on top of gate dielectrics, the effective dielectric constant $\varepsilon_{r,eff} \approx 2.2$ has been used, to take into account that nanowires are not embedded in the SiO_2 layer.[38]

The transfer characteristics of a typical InAs NW FET are shown in Figure 2 and demonstrate n-type transport, with full depletion of the FET channel achievable at V_{sg} from -60 to -40 V, and full accumulation of the FET at V_{sg} from 60 to 100 V. Switching the transistor between ON and OFF states (accumulation/depletion) provides InAs nanowire FETs on/off current ratio of ~10^3. The transconductance is plotted in the inset (of Figure 2a), and its peak value is ≈ 6 µS at V_{sg}= 0 V and V_{sd}= 20 mV. Also, from the linear part of the sub-threshold region of the transfer plot, the sub-threshold swing, $SS \equiv (\frac{\partial log I_{sd}}{\partial V_{sd}})^{-1}$, is approximately 10 V/dec. By using equations

(1-2) field-effect mobility was estimated to be ~300 $cm^2V^{-1}s^{-1}$. The output characteristics of InAs nanowire FETs (Figure 2b) exhibit linear behavior over the entire source-drain voltage measurement range, confirming the Ohmic properties of the contacts. The FET ON-state resistance was estimated to be ≈ 50 Ω from the inverse gradient of the I-V curve (V_{sg}=100 V), demonstrating I_{sd} of 2 mA at V_{sd} of 100 mV.

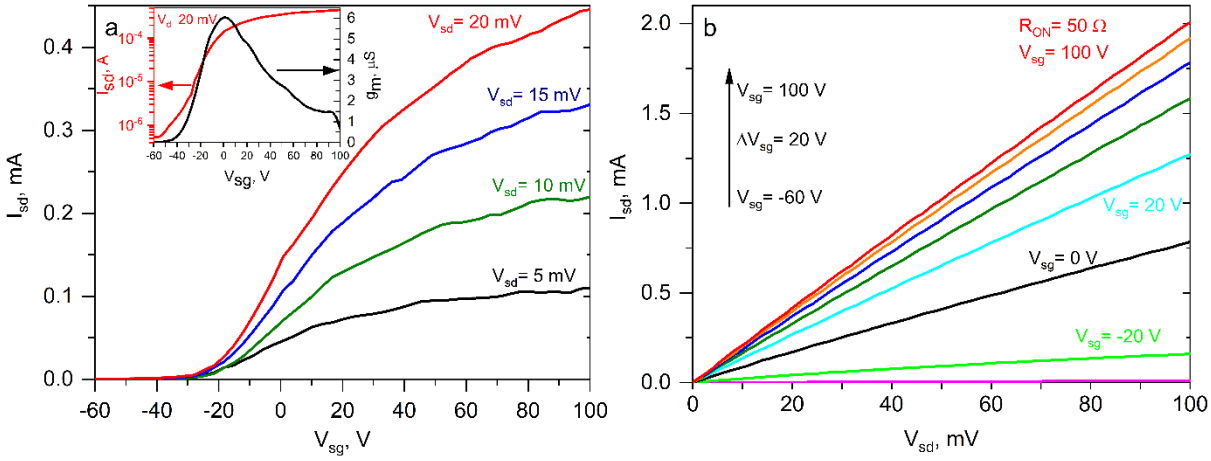

Figure 2. ***a)*** *DC transfer characteristics of the assembled InAs nanowire-based switch, on a linear scale. Inset shows FET characteristics on a log-linear scale (red line) and transconductance vs gate voltage (black line).* ***b)*** *DC output characteristics of the NW-based FET switch, with 50 Ohm device resistance obtained in full accumulation regime (Vsg=100V).*

2.4. InAs NW FETs switch RF/microwave performance

The same FET devices were then used for microwave characterization (Experimental Section). Initially, to evaluate the possible influence of the highly doped p^{++}-Si substrate (resistivity of 0.1 Ω cm), S-parameters of the CPW with full transistor geometry, but without semiconducting nanowires were performed. The back gate (p^{++}-Si) was biased at the same levels as during FET tests. The measurements confirmed that at -60, 0 and 100 V gate bias, the S-parameters of the structures, without nanowires, do not show any detectable changes. (Supplementary Information). Thus, it was concluded that biasing effects of the conducting Si common gate can be neglected.

S-parameters of the InAs NW FET devices were measured up to 33 GHz and the results are presented in Figure 3. Reflection, S_{22} (Figure 3a), and transmission, S_{21} (Figure 3b), coefficients in dB-scale represent the operation of the switch at high frequencies. Both the reflection and transmission coefficients change significantly when the switch is closed (negative V_{sg}) and open (positive V_{sg}). When the gate bias is negative (FET is depleted), the resistance of the nanowires is two orders of magnitude larger than the characteristic impedance and it should not affect S-parameters. Indeed, when the gate bias is negative: (i) transmission remains high, giving S_{21} in the range between -4 dB and -2 dB; (ii) reflection remains low with S_{22} below -20 dB; (iii) S-parameters do not change at V_{sg} of -60, -40 and -20 V. It indicates that signal is transmitted and the switch is closed. Note that the resistance is estimated to be ≈128 Ω when gate bias is zero (calculated as an inverse gradient of the I-V curve at V_{sg}= 0 V), and S-parameters did not change significantly as compared to the closed switch conditions.

The behavior of S-parameters changes when V_{sg} is more positive - transmission decreases and reflection increases, turning the switch into an open state. The strongest effect happens at V_{sg} =100 V when the channel resistance is ≈50 Ω, *i.e.* S_{21} drops by 7-10 dB, indicating low transmission, and S_{22} varies between -13 dB and -6 dB, indicating an increase in reflection.

In regards to the range of gate voltages producing the majority of switching effect, it was observed that relatively modest voltages, V_{sg} ~ -5V were sufficient to keep the switch in the closed state, to allow microwave transmission, whereas positive gate voltage at the level of ~60V have provided strong reflection characteristics, corresponding to the switch open state. Additional modelling using *Sonnet EM* planar electromagnetic simulator based on method-of-moments have shown that currently used 1.5μm thickness of SiO_2 gate dielectric can be reduced to 0.3μm thickness, without sacrificing the performance of the switch. Such 5-fold dielectric thickness reduction is expected to bring about corresponding decrease of gate voltages to 15-

20V level.

S-parameters of the switch can be described by a transmission line model having an additional variable shunt admittance (Figure 3f), *i.e.* the NWs between the signal and ground lines of the CPW add a shunt admittance, Y_{NW}. This admittance is composed of the NW conductance and associated inductance. Hence, $Y_{NW} = G_{NW} - i/\omega L_{NW}$, where G_{NW} and L_{NW} are the distributed conductance and inductance, respectively, whose values are controlled by the gate bias applied to the NW FETs. The characteristic impedance, Z_0, and propagation constant, γ, of the CPW line, with the nanowires, can be defined as: [39]

$$Z_0 = \sqrt{\frac{Z}{Y+Y_{\mathrm{NW}}}} \tag{3}$$

$$\gamma = \alpha + i\beta = \sqrt{Z(Y + Y_{\mathrm{NW}})} \tag{4}$$

where $Z = R + i\omega L$ and $Y = G + i\omega C$, R, L, G and C are the distributed resistance, inductance, conductance, and capacitance of the unloaded CPW (per unit length), α and β are attenuation and phase constant, respectively. The attenuation is the loss in the transmission line as the electromagnetic wave propagates and Z_0 is the characteristic impedance. Both Z_0 and α can be calculated from S-parameters via ABCD parameters[39] as described in Supporting Information.

Using Equations (S6) and (S7), (Supporting Information), α and Re(Z_0) are plotted in Figure 3(c,d). As the gate bias is increased and positive (FET is 'on') InAs NWs channel becomes more conductive, *i.e.* the shunt conductance G_{NW} increases. This gives rise to an increased attenuation constant, indicating an increase in loss associated with NWs. Therefore, the transmission coefficient, S_{21}, decreases. Furthermore, according to Equation (3), Z_0 also changes resulting in a mismatch with the nominal 50 Ω at the reference plane, and therefore input reflection of the switch, S_{11}, will increase; which further decreases the signal that passed through the switch.

It is interesting to determine the values of the NW conductance, G_{NW}, and inductance, L_{NW} at microwave frequencies. These values can be obtained by noting that:

$$Z_0\gamma = Z \tag{5}$$

$$\frac{\gamma}{Z_0} = Y + Y_{NW} \tag{6}$$

We see from equation (6) that the ratio γ/Z_0 gives the sum of the unloaded distributed shunt admittance of the CPW transmission line, Y, and the additional contribution from the NWs, Y_{NW}. The value of Y can be determined by measuring the CPW with no NWs (or this case, the CPW line with NWs but very large negative V_{sg} - resulting in $Y_{NW}=0$). The value of Y then follows from equation (6) with $Y_{NW}=0$ and equations (S6) and (S7). The measurements are then repeated for a CPW line with NWs resulting in γ/Z_0 from equation (6). Therefore, if we find the difference between these loaded and unloaded values we can determine the additional distributed NW admittance:

$$Y_{NW} = G_{NW} - i\frac{1}{\omega L_{NW}} = \frac{\gamma}{Z_0} - Y \tag{7}$$

Figure 3 (e) shows the extracted values of G_{NW} using equations (S6) and (S7) (Supporting Information) and equation (7). It is seen that the NW conductance varies from approximately 0.06 S mm^{-1} for V_{sg} = 100 V reducing to a figure of 0.005 S mm^{-1} for V_{sg} = 0V. Although not plotted for brevity, the inductance varies from 0.5 nH mm at V_{sg}=100 V up to 1.5 nH mm at V_{sg}=20 V. Note that the unusual units of nH mm arise from the fact that the shunted NW admittance in equation (7), Y_{NW}, has units of S mm^{-1}. There is a frequency dependence for G_{NW} and L_{NW}, with G_{NW} decreasing with frequency and L_{NW} increasing, as is in the case of a conducting wire due to the skin effect. The imaginary component of Y_{NW}, due to L_{NW}, is comparable in magnitude to the real part G_{NW} at lower frequencies; however, due to the $1/\omega$ dependence, it becomes insignificant at 33 GHz. This explains the increase in Re(Z_0) for

positive V_{sg} as the frequency increases.

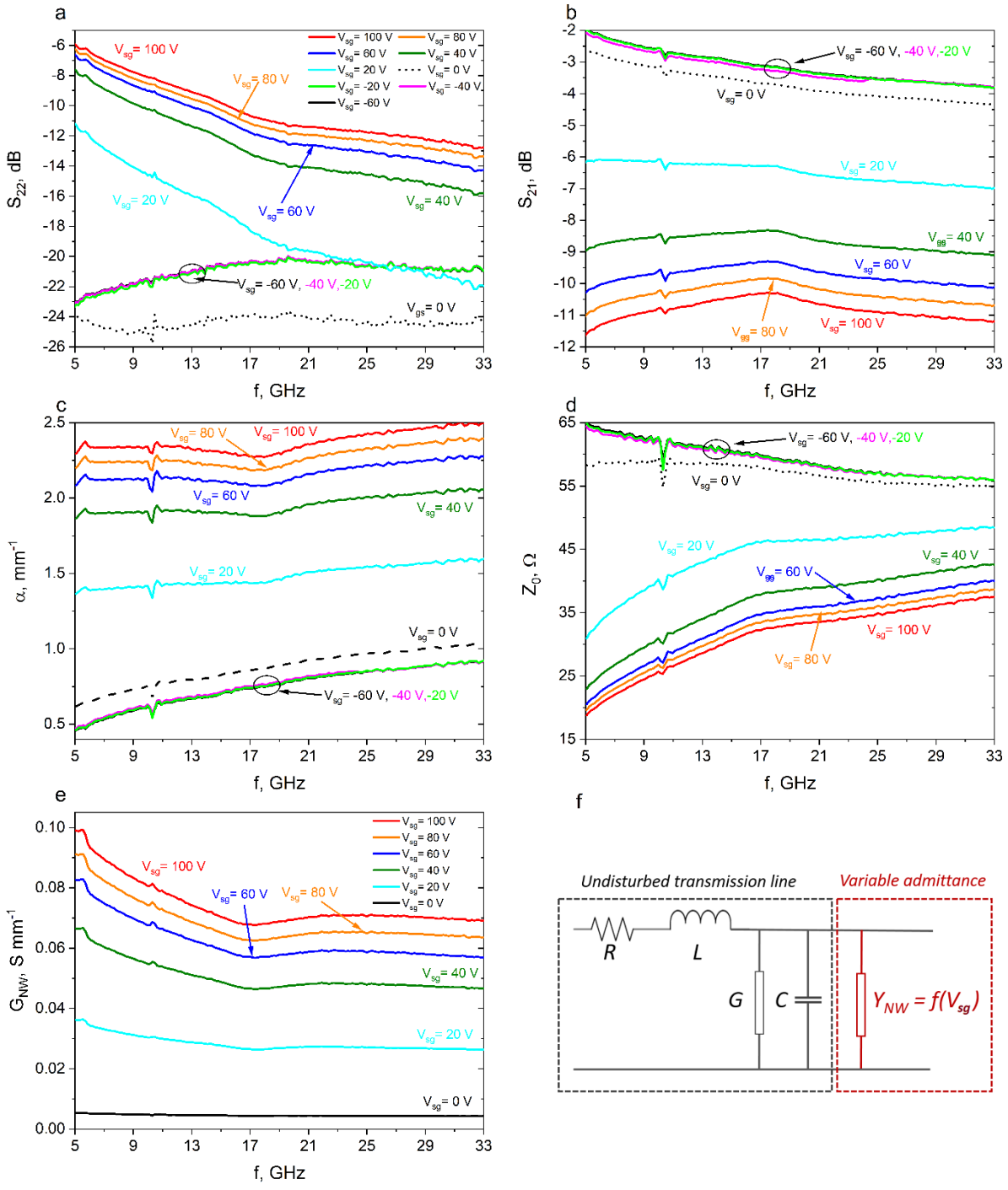

Figure 3 ***a,b****) Reflection coefficient S_{22} and transmission coefficient S_{21} in dB scale at different V_{sg} from -60 V to 100 V with a step of 20 V. Representation of the S-parameters in dB follows the formula $S_{ij}[dB]=20\log S_{ij}$.where i,j are 1 or 2;.* ***c,d****) Attenuation, α, and Re(Z_0), calculated from S-parameters at respective V_{sg}.,* ***e****) Effective distributed NW conductance,* ***f****) Equivalent circuit diagram of CPW InAs NW switch.*

Finally, the switch performance was demonstrated in an offset-open configuration that can be employed in a reconfigurable matching circuit based on single-stub tuning, thus providing additional capabilities for the design of reconfigurable microwave circuits based on phase shift. The devices were implemented by assembling InAs nanowires at the terminating end of the CPW and have demonstrated very good performance with nanowire FET providing a variable resistive load ranging from 33 Ω to 1.67 kΩ, resulting in the phase shift of 180° at 3 GHz. (Supporting Information)

3. Conclusions

In summary, solution processable InAs nanowire bottom-gated FETs were demonstrated as microwave switches working in the frequency range of 5 to 33 GHz. The large number of NWs, assembled in shunt configuration by dielectrophoresis, has enabled tuning of the overall resistance by 3 orders of magnitude from ~50 Ω to ~50 kΩ, where 50 Ω NW FET resistance is the lowest reported among solution processed or direct transferred, planar NW FETs with low-k gate-dielectric[40], to the best of the authors' knowledge. For instance, solution processed multi-NW ZnO FETs with 300 nm thick parylene top-gate dielectric demonstrated ON-resistance of ≈ 0.5 MΩ[37], whereas bottom-gated Si NWs with 250 nm thick SiO_2 dielectric exhibited ON-resistance of 13 kΩ.[34] Dense arrays of InAs NW FET with transfer printed nanowires on flexible substrate with ~8 nm thick Al_2O_3 gate dielectric demonstrated ON-resistance of 1 kΩ with ON/OFF ratio[41] 10 times lower than the one reported in this work. In general, the majority of high-frequency III-V and, especially, InAs multi-NW FETs reported in the literature, are vertical structures[42] fabricated by non-printed electronics deposition techniques.

The RF/microwave characterization of the switches demonstrated the difference in transmission and reflection coefficients between closed and open states of the switch to be 7-10 dB and 6-13

dB, respectively, though there were losses related to the p^{++}-Si/SiO_2 substrate and thin, narrow conductors of the CPW. An isolation of around 10 dB is considered to be sufficient for reconfigurable devices, whereas microwave and millimeter-wave operation of the switches is particularly attractive for reconfigurable antennas/surfaces for wireless communications and IoT,[43] space applications, remote sensing, surveillance and beam-forming circuits.[44] FET switch design offers several advantages, including very low power consumption as compared to PIN diodes,[45] fast switching times and normal temperature operation as compared to phase-change temperature tunable switches (GeTe and VO_2).[46]

Finally, we demonstrated the switch in offset-open geometry, where it played the role of a phase shifter with a maximum phase shift of 180° at 3 GHz.

To conclude, further improvements of InAs NWs FET microwave/mm-wave switches can be gained by replacing lossy silicon with low-loss plastic substrates and thinner low-k polymeric dielectrics to push up operating frequency range while reducing operating voltages and to move towards truly flexible electronics.

4. Experimental Section

Nanowires growth and dispersions preparation: The InAs nanowires were grown via the vapor-liquid-solid mechanism using 30 nm diameter Au nanoparticles dispersed from a commercial colloidal Au solution on a poly-L-lysine treated InAs(111)B substrate by metal-organic vapor phase epitaxy (MOVPE). Growth was conducted in an Aixtron 200/4 reactor at 100 mbar hydrogen atmosphere with total flow rate of 15 slm, using trimethylindium and arsine as precursors. The nanowires were grown at 597 ºC for 60 min with a V/III ratio of 1.6 after 10 min of annealing at 650 ºC to remove the substrate native oxide and allow for alloying between the gold droplet and indium from the substrate. These conditions provided excellent growth

yield, <111>B nanowire growth direction, and mainly stacking fault-free wurtzite crystal structure.[35]

Nanowires dispersions were obtained by sonicating as-grown InAs NWs in anisole to detach NWs from the host substrate. Typical length of the nanowires in the dispersion was 5-7 microns.

Positive photolithography and lift-off technique were used for fabrication of metal tracks on the substrate. Bi-layer technique of PMGI SF6 and S1805 photoresists was used.

Bottom electrodes for DEP: Auxiliary Al bottom electrodes, 20nm thick, for dielectrophoresis, were structured by photolithographic lift-off technique.

DEP was performed on an inclined substrate.[34] Sinusoidal signal of 10 kHz, 20 V_{p-p} was applied to Al device electrodes, and nanowires formulation was drop-casted on top. DEP was conducted for 30 sec. Excessive nanowires and clusters of nanowires were removed by quick device sonication in IPA.

Top electrodes and sulfurization of the contacts: Before top-electrode deposition, nanowires under the contact area were treated with ammonium polysulfide solution for 10 min at 40 °C. The solution was prepared[47] by adding of 150 µl of 20-25% water solution of $(NH_4)_2S$ and 50 µl of S-saturated $(NH_4)_2S_x$ into 200 ml of DI water. The saturated component was prepared by adding 3 g of sulfur powder into 30 ml of 20-25% $(NH_4)_2S$. Sulfurization process was stopped by rinsing the samples in DI water. Top contacts (Ti/Au), 150 nm thick, were deposited by e-beam evaporation and structured by lift-off technique.

Microwave characterization: Two-port S-parameters measurements were performed using a Keysight N5247A PNA-X network analyzer, MPI TS-2000 SE probe station, and two MPI Titan 26 GHz GSG probes both having a 150 µm pitch, used to contact the fabricated CPW switch. The shielded environment of the probe station was purged with nitrogen and kept at room temperature during the measurements. Measurements were performed from 5 to 33 GHz,

at an input power of -10 dBm. Weak microscope illumination was used to observe the positioning the probes. No influence of microscope light was observed on either DC or frequency response of the devices. On-wafer multiline thru-reflect-line (mTRL) calibration was performed to move the reference plane of the measurement to the CPW switches (end of the tapered lines). The standards used for the calibration were a zero-length 'thru', a 'reflect' and two 'lines' with lengths of 1350 μm (covering 5-26 GHz) and 450 μm (covering 25-65 GHz), in order to cover the desired frequency range. One additional 'line' structure of 2200 μm was built to cover frequencies between 3 and 24 GHz for the offset-open. The source-drain DC bias (Agilent 2902B) was applied to the devices through one of the bias tees of the VNA and one of the two GSG probes, whereas the gate DC bias was applied through an MPI Kelvin probe.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the corresponding author.

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References

[1] G. A. T. Sevilla, M. M. Hussain, *IEEE J. Emerg. Sel. Top. Circuits Syst.* **2017**, *7*, 147.

[2] D. Sette, A. Blayo, C. Poulain, D. Mercier, in *2013 IEEE MTT-S Int. Microw. Symp. Dig.*, IEEE, **2013**, pp. 1–4.

[3] W. G. Whittow, A. Chauraya, J. C. Vardaxoglou, Y. Li, R. Torah, K. Yang, S. Beeby, J. Tudor, *IEEE Antennas Wirel. Propag. Lett.* **2014**, *13*, 71.

[4] M. Y. Chen, X. Lu, H. Subbaraman, R. T. Chen, in *Proc. SPIE - Int. Soc. Opt. Eng.* (Eds.: T. George, M.S. Islam, A.K. Dutta), Omega Optics Inc., 10435 Burnet Rd STE 108, Austin, TX 78758, United States, **2009**, p. 731814.

[5] W. G. Whittow, Y. Li, R. Torah, K. Yang, S. Beeby, J. Tudor, *Electron. Lett.* **2014**, *50*, 916.

[6] R. D. Seager, A. Chauraya, J. Bowman, M. Broughton, R. Philpott, N. Nimkulrat, *Electron. Lett.* **2013**, *49*, 1507.

[7] S. M. Saeed, C. A. Balanis, C. R. Birtcher, *IEEE Antennas Wirel. Propag. Lett.* **2016**, *15*, 1979.

[8] M. Y. Chen, D. Pham, H. Subbaraman, X. Lu, R. T. Chen, *IEEE Trans. Microw. Theory Tech.* **2012**, *60*, 179.

[9] J. G. D. Hester, M. M. Tentzeris, *IEEE Trans. Microw. Theory Tech.* **2016**, *64*, 4763.

[10] A. Traille, A. Georgiadis, A. Collado, Y. Kawahara, H. Aubert, M. M. Tentzeris, in *2014 XXXIth URSI Gen. Assem. Sci. Symp. (URSI GASS)*, IEEE, **2014**, pp. 1–4.

[11] C. C. Sun, H. T. Chou, *2016 IEEE Int. Symp. Radio-Frequency Integr. Technol.* **2016**, 1.

[12] N. F. M. Aun, P. J. Soh, A. A. Al-Hadi, M. F. Jamlos, G. A. E. Vandenbosch, D. Schreurs, *IEEE Microw. Mag.* **2017**, *18*, 108.

[13] J. T. Bernhard, *Synth. Lect. Antennas* **2007**, *2*, 1.

[14] Y. Yashchyshyn, in *Perspect. Technol. Methods MEMS Des. 2009. MEMSTECH 2009. 2009 5th Int. Conf.*, **2009**, pp. 155–157.

[15] M. A. M. Leenen, V. Arning, H. Thiem, J. Steiger, R. Anselmann, *Phys. Status Solidi Appl. Mater. Sci.* **2009**, *206*, 588.

[16] S. Mandal, Y.-Y. Noh, *Semicond. Sci. Technol.* **2015**, *30*, 064003.

[17] L. Qian, W. Xu, X. Fan, C. Wang, J. Zhang, J. Zhao, Z. Cui, *J. Phys. Chem. C* **2013**, *117*, 18243.

[18] P. H. Lau, K. Takei, C. Wang, Y. Ju, J. Kim, Z. Yu, T. Takahashi, G. Cho, A. Javey, *Nano Lett.* **2013**, *13*, 3864.

[19] M. Ha, J.-W. T. Seo, P. L. Prabhumirashi, W. Zhang, M. L. Geier, M. J. Renn, C. H. Kim, M. C. Hersam, C. D. Frisbie, *Nano Lett.* **2013**, *13*, 954.

[20] G. Eda, M. Chhowalla, *Nano Lett.* **2009**, *9*, 814.

[21] S. Wang, P. J. Chia, L. L. Chua, L. H. Zhao, R. Q. Png, S. Sivaramakrishnan, M. Zhou, R. G. S. Goh, R. H. Friend, A. T. S. Wee, P. K. H. Ho, *Adv. Mater.* **2008**, *20*, 3440.

[22] G. Eda, G. Fanchini, M. Chhowalla, *Nat. Nanotechnol.* **2008**, *3*, 270.

[23] X. Liu, Y.-Z. Long, L. Liao, X. Duan, Z. Fan, *ACS Nano* **2012**, *6*, 1888.

[24] N. P. Dasgupta, J. Sun, C. Liu, S. Brittman, S. C. Andrews, J. Lim, H. Gao, R. Yan, P. Yang, *Adv. Mater.* **2014**, *26*, 2137.

[25] S. A. Dayeh, D. P. R. Aplin, X. Zhou, P. K. L. Yu, E. T. Yu, D. Wang, *Small* **2007**, *3*, 326.

[26] S. A. Dayeh, *Semicond. Sci. Technol.* **2010**, *25*, DOI 10.1088/0268-1242/25/2/024004.

[27] M. Berg, J. Svensson, E. Lind, L.-E. Wernersson, *Appl. Phys. Lett.* **2015**, *107*, 232102.

[28] D. B. Suyatin, C. Thelander, M. T. Björk, I. Maximov, L. Samuelson, *Nanotechnology* **2007**, *18*, 105307.

[29] F. Leonard, A. A. Talin, *Nat Nano* **2011**, *6*, 773.

[30] Q. Hang, F. Wang, P. D. Carpenter, D. Zemlyanov, D. Zakharov, E. A. Stach, W. E. Buhro, D. B. Janes, *Nano Lett.* **2008**, *8*, 49.

[31] D. Liang, J. Du, X. P. A. Gao, *J. Mater. Sci. Technol.* **2015**, *31*, 542.

[32] E. Halpern, G. Elias, A. V Kretinin, H. Shtrikman, Y. Rosenwaks, *Appl. Phys. Lett.* **2012**, *100*, 262105.

[33] S. Johansson, E. Memisevic, L. E. Wernersson, E. Lind, *IEEE Electron Device Lett.* **2014**, *35*, 518.

[34] M. Constantinou, G. P. Rigas, F. A. Castro, V. Stolojan, K. F. Hoettges, M. P. Hughes, E. Adkins, B. A. Korgel, M. Shkunov, *ACS Nano* **2016**, *10*, 4384.

[35] H. J. Joyce, J. Wong-Leung, Q. Gao, H. H. Tan, C. Jagadish, *Nano Lett.* **2010**, *10*, 908.

[36] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, J. L. Goldman, *Nature* **2003**, *425*, 274.

[37] C. Opoku, K. F. Hoettges, M. P. Hughes, V. Stolojan, S. R. P. Silva, M. Shkunov, *Nanotechnology* **2013**, *24*, 405203.

[38] O. Wunnicke, *Appl. Phys. Lett.* **2006**, *89*, 83102.

[39] B. Shao, R. Weerasekera, L.-R. Zheng, R. Liu, W. Zapka, P. Lindberg, in *2008 12th IEEE Work. Signal Propag. Interconnects*, IEEE, **2008**, pp. 1–4.

[40] X. Duan, *IEEE Trans. Electron Devices* **2008**, *55*, 3056.

[41] T. Takahashi, K. Takei, E. Adabi, Z. Fan, A. M. Niknejad, A. Javey, *ACS Nano* **2010**, *4*, 5855.

[42] E. Lind, *Semicond. Sci. Technol.* **2016**, *31*, 093005.

[43] M. Agiwal, A. Roy, N. Saxena, *IEEE Commun. Surv. Tutorials* **2016**, *18*, 1617.

[44] W.-T. Fang, C.-H. Chen, Y.-S. Lin, *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 3950.

[45] A. Chakraborty, B. Gupta, *IEEE Microw. Mag.* **2017**, *18*, 22.

[46] M. Wang, F. Lin, M. Rais-Zadeh, *IEEE Microw. Mag.* **2016**, *17*, 70.

[47] S. Nadar, C. Rolland, J.-F. Lampin, X. Wallart, P. Caroff, R. Leturcq, *Nano Res.* **2015**, *8*, 980.