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Research Article

Design of 0.8–2.7 GHz High Power Class-F Harmonic-Tuned Power Amplifier with Parasitic Compensation Circuit

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The design, implementation, and measurements of a high efficiency and high power wideband GaN HEMT power amplifier are presented. Package parasitic effect is reduced significantly by a novel compensation circuit design to improve the accuracy of impedance matching. An improved structure is proposed based on the traditional Class-F structure with all even harmonics and the third harmonic effectively controlled, respectively. Also the stepped-impedance matching method is applied to the third harmonic control network, which has a positive effect on the expansion bandwidth. CGH40025F power transistor is utilized to build the power amplifier working at 0.8 to 2.7 GHz, with the measured saturated output power 20–50 W, drain efficiency 52%–76%, and gain level above 10 dB. The second and the third harmonic suppression levels are maintained at −16 to −36 dBc and −16 to −33 dBc, respectively. The simulation and the measurement results of the proposed power amplifier show good consistency.

1. Introduction

With the rapid development of wireless communication technology, the requirement of speed and frequency resource of communication is increasing dramatically [1]. For example, in the fourth-generation mobile communication technology, radio frequency power amplifiers used in base stations are expected to have high performances such as high efficiency and high output power. In order to improve the energy efficiency and signal coverage area of communication systems, efficiency and output power of power amplifier have been a hot topic since 2000 years [2–4]. At the same time, so as to cover more carriers' operating frequency bands, power amplifiers are required to have good performances of broadband. Thus, the importance of power amplifier as the most critical module in a communication system is self-evident.

Harmonic tuning is one of key technologies to improve the efficiency and output power. Various operation classes such as Class-E [5], Class-F [6], and inverse Class-F [7] have been proposed. In particular, the Class-F operation has attracted attention due to its excellent performance [8]. A typical circuit model of Class-F power amplifier is shown in Figure 1 in which the Cout and Lout represent package parasitic effects of the transistor.

The output voltage and current of the transistor in time domain can be expressed as follows:

$$I_d(t) = I_0 + \sum_{n=1}^{\infty} I_n \cdot \cos(n\omega t + \xi_n)$$
$$V_{ds}(t) = V_{DD} - \sum_{n=1}^{\infty} V_n \cdot \cos(n\omega t + \psi_n), \quad (1)$$

where n is the order of the harmonics and ξ_n and ψ_n are the phases of the output current and voltage at the nth order, respectively. The current and voltage are both related to the impedance at a certain frequency. The impedance of each harmonic can be expressed as

$$Z_{L\cdot n} = \frac{V_n}{I_n} \cdot e^{j\phi_n}, \quad (2)$$

where $\phi_n = \psi_n - \xi_n$.

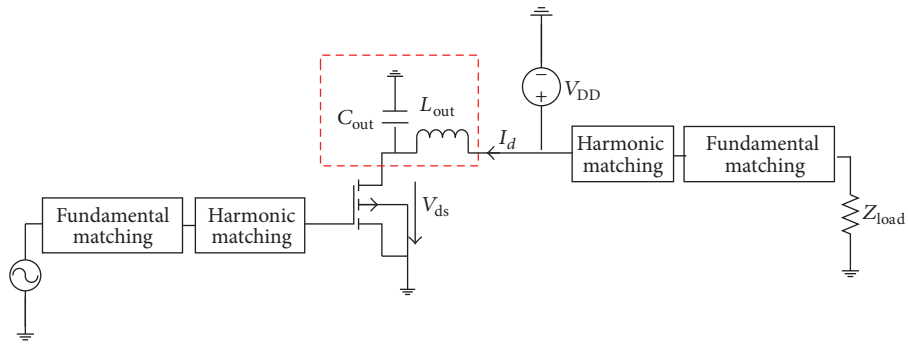

Figure 1: Circuit diagram of a Class-F power amplifier model.

Table 1: Comparison with the state-of-the-art broadband power amplifiers.

Ref.	Bandwidth (GHz) (%)	Power (dBm)	Gain (dB)	DE (%)
[10]	0.5–1.8, 113	39–40.8	9–10.8	50–69
[11]	1.0–2.9, 97	>39.3	>10.3	>56.8
[12]	1.9–4.3, 78	40–41.8	9–11	57–72
[13]	1.4–2.7, 63	41 (around)	9 (around)	68 (average)
This work	0.8–2.7, 109	43–47	10–14	52–76

According to the theory of Class-F power amplifiers [9], high efficiency and high output power can be anticipated when the impedance of all even harmonics is matched to zero, odd harmonics to infinite, and the fundamental to 50 Ω. However, it is extremely difficult to achieve the above requirements in real practices because of the existence of infinite orders of harmonics and the shift of the fundamental impedance caused by the parasitic effects of the package. The further analysis will focus on improving these two aspects in order to boost the performance of Class-F power amplifiers.

A new architecture has been proposed to compensate the parasitic effects of package and improve the harmonic control ability of the power amplifier. Using CGH40025F transistor, we designed a power amplifier with the proposed architecture, which operates in range from 0.8 to 2.7 GHz with a relative bandwidth of 109%. The designed power amplifier realizes saturated output power of over 43 dBm and average drain efficiency greater than 60%. The recent broadband power amplifier research works are listed in Table 1. It is obvious that this work has made great progress compared with the previous works which have been published in terms of output power, drain efficiency, frequency of operation, and gain across the whole frequency band.

2. Analysis and Design of Class-F Power Amplifier

2.1. Parasitic Effect Compensation. As the frequency goes higher, the parasitic effect becomes increasingly nonnegligible. Ignoring package parasitic effect will cause the mismatch of the transistor's output impedance. The control of the fundamental impedance is given first priority to minimize the impedance mismatch since the fundamental is the main output signal.

The conventional circuit of the transistor and the corresponding harmonic control network is shown in Figure 2(a) [14]. The novel structure is proposed as depicted in Figure 2(b). With full consideration of the actual package effect (L_{out} and C_{out}), the improvement of the circuit (introducing compensation circuit TL4, TL5, and TL6) is presented so that package parasitic effect is alleviated at the fundamental frequency to a certain extent.

In the theoretical derivation of this Class-F power amplifier, the ideal reference plane is the voltage-controlled current source surface of the power transistor (Figure 2(a)). But the output pin can only reach the package plane (green dashed box) due to the physical limits of the actual package (Figure 2(b)). This position deviates from the ideal reference plane, introducing parasitic effects into actual model.

Microstrip lines TL4, TL5, and TL6 are used to adjust the electrical length and characteristic impedance so that the actual transistor's output impedance is close to the ideal output impedance without packaging. It can be observed that the measured transistor output impedance with parasitic effect (black curve) can be shifted to the compensated impedance (blue curve) by adding parasitic regulation, which is closer to the ideal simulated impedance (red curve) as illustrated in Figure 3. A measured comparison between before and after parasitic compensation is given in Figure 4. One can see that both drain efficiency and output power increase after the addition of the parasitic compensation circuit. Clearly the parasitic effect is reduced so that the fundamental impedance matching can be realized better by this design.

2.2. High-Order Harmonics Suppression. According to Figure 2(a), a conventional Class-F power amplifier by employing a high-Q harmonic control network is observed, which can only match harmonics up to the third order. This traditional harmonic control network severely limits the bandwidth as well as the ability to control higher order harmonics; hence, it affects the efficiency and output power of Class-F power amplifiers greatly [15, 16].

An improved harmonic control network design is proposed in Figure 2(b). Originating from the principle of quarter-wave impedance transformation, the input

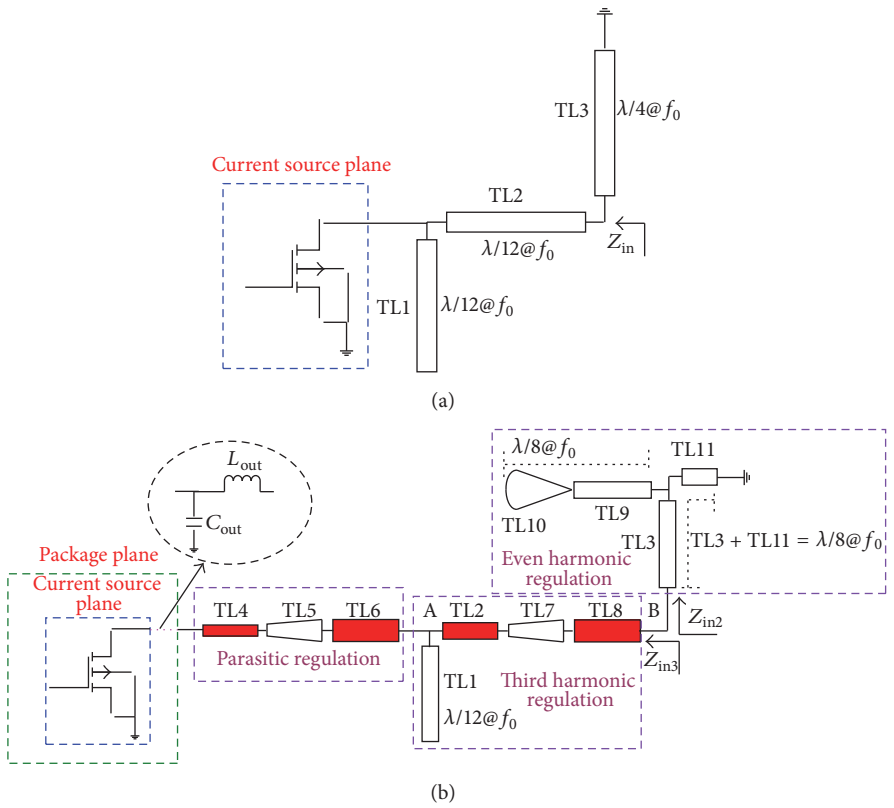

FIGURE 2: Circuit design of (a) conventional and (b) improved harmonic control network.

impedance of the shorted-terminal TL11 combined with TL3 can be expressed as

$$Z_{4m} = jZ_{3,11} \tan\left[\frac{\pi}{4}\frac{f_{4m}}{f_0}\right] \quad m = 1, 2, 3, \ldots, \tag{3}$$

where $Z_{3,11}$ is the characteristic impedance of TL3 and TL11, f_{4m} is the $(4m)$th harmonic, and f_0 is the fundamental frequency.

The radial line stub TL10 can maintain the same impedance characteristics over a wide bandwidth. The total electrical length of TL10 and TL9 is chosen to be $\lambda/8$ (λ is the wavelength of the fundamental). The input impedance of the open-terminal TL10 combined with TL9 can be approximately expressed as

$$Z_{4m-2} = -j\frac{Z_{9,10}}{\tan\left[(\pi/4)\left(f_{4m-2}/f_0\right)\right]} \quad m = 1, 2, 3, \ldots, \tag{4}$$

where $Z_{9,10}$ is the characteristic impedance of TL9 and TL10 and f_{4m-2} is the $(4m-2)$th harmonic. The input impedance Z_{in2} can be obtained from (3) and (4)

$$Z_{\text{in2}} = \begin{cases} Z_{4m-2} = 0 \\ Z_{4m} = 0 \end{cases} \quad m = 1, 2, 3, \ldots. \tag{5}$$

As seen from (5), the impedance at all even-order harmonics is matched to zero.

Considering the difficulty of matching and the limited area of the circuit layout, the odd harmonics are matched to the third order. Stepped-impedance matching technique is applied to harmonic control networks of Class-F power amplifier, which greatly reduces quality factor of the resonant network. The microstrip lines TL2, TL7, and TL8 are added to the harmonic network as adjusting auxiliary lines. Together with TL1, the third harmonic is suppressed. For TL1, the input impedance at point A can be expressed as

$$Z_A = -j\frac{Z_1}{\tan\left[(\pi/6)\left(f_3/f_0\right)\right]}, \tag{6}$$

where Z_1 is the characteristic impedance of TL1 and f_3 is the third harmonic. Z_A holds zero for the third harmonic. The input impedance Z_{in3} can be expressed as

$$Z_{\text{in3}} = jZ_8\frac{Z_2\tan\left[6\pi/n_1\right] + Z_8\tan\left[6\pi/n_2\right]}{Z_8 - Z_2\tan\left[6\pi/n_1\right]\tan\left[6\pi/n_2\right]}. \tag{7}$$

Z_2 and Z_8 are the characteristic impedance of TL2 and TL8, respectively. TL7 is the stepped-impedance line to reduce reflection caused by impedance mismatch. Theoretically when the total electrical length of TL2 and TL8 equals $\lambda/12$, the impedance of third harmonic is well maintained at high impedance region over a certain frequency range, which requires $\lambda/n_1 + \lambda/n_2 \approx \lambda/12$. λ/n_1 and λ/n_2 are the electrical lengths of TL2 and TL8, respectively.

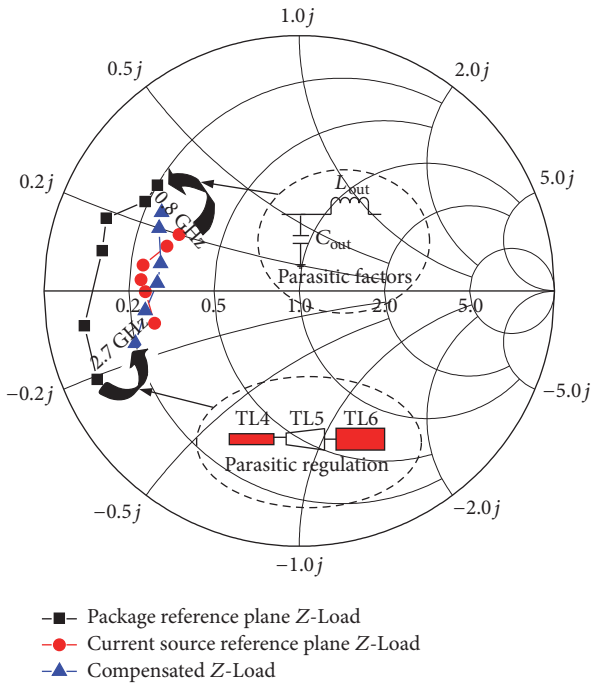

FIGURE 3: Parasitic compensation of fundamental impedance.

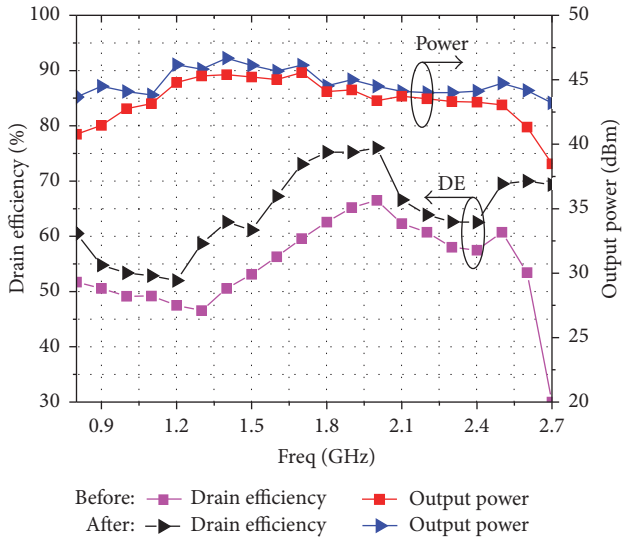

FIGURE 4: Measured drain efficiency and the output power before and after parasitic compensation.

The newly proposed Class-F power amplifier topology (Figure 2(b)) is superior to the conventional structure (Figure 2(a)) in the sense that all even harmonics can be matched to zero and the impedance of the harmonics is controlled at a much broader frequency band (even harmonics are kept at low impedance and the third harmonic is kept at high impedance).

The simulated impedance of the second harmonic (1.6–5.4 GHz) and the third harmonic (2.4–8.1 GHz) are shown in Figure 5 for both topologies. Compared to the conventional structure, the new structure demonstrates that the

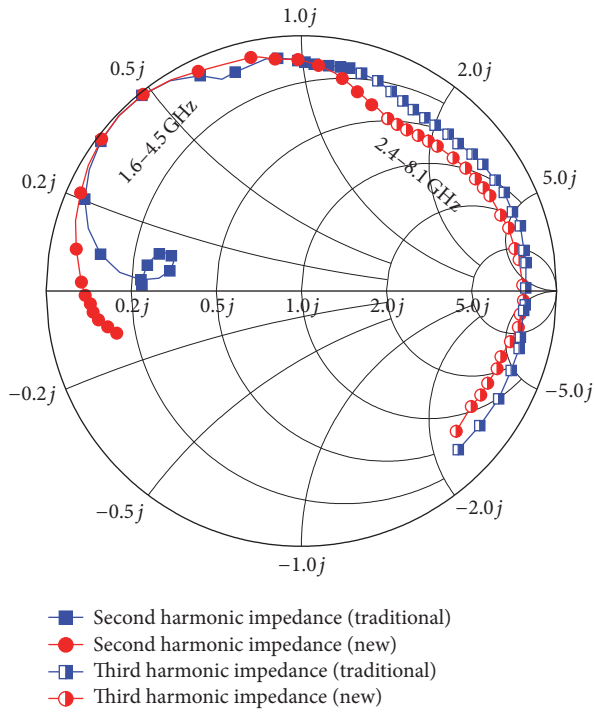

FIGURE 5: Simulated second and third harmonics impedance for conventional and improved structures.

impedance of the second harmonic and the third harmonic is better maintained in the low impedance zone and high impedance zone over the whole frequency band, respectively.

Drain current and voltage simulations for the two different topologies are displayed in Figures 6(a) and 6(b), respectively. It can be observed that the overlap of the drain current and the voltage waveform in the new topology is reduced, and therefore the efficiency and output power of the new topology get higher.

Harmonic control network is also added to the input. The impedance of the second and third harmonics is matched to zero and infinite, respectively. The fundamental impedance of the input and the output needs to be matched to 50 Ω. The final schematic of designed power amplifier is presented in Figure 7.

3. Fabrication and Measurement Results

The transistor adopted in this work is CGH40025F, which is a GaN HEMT from Cree Company. The broadband power amplifier was implemented on a Rogers substrate with the dielectric constant of 3.66 and thickness of 0.762 mm, as shown in Figure 8. The gate bias is set as −2.7 V. Setting the drain voltage at 32 V instead of the typically suggested 28 V provides a higher output power at the expense of efficiency. Measurements were made using a continuous wave. The measurement and simulation results of output power, drain efficiency, power added efficiency (PAE), and gain are in good agreement as illustrated in Figures 9 and 10, respectively. The measured saturated output power is between 43 dBm and 47 dBm from 0.8 to 2.7 GHz giving a bandwidth of 109%.

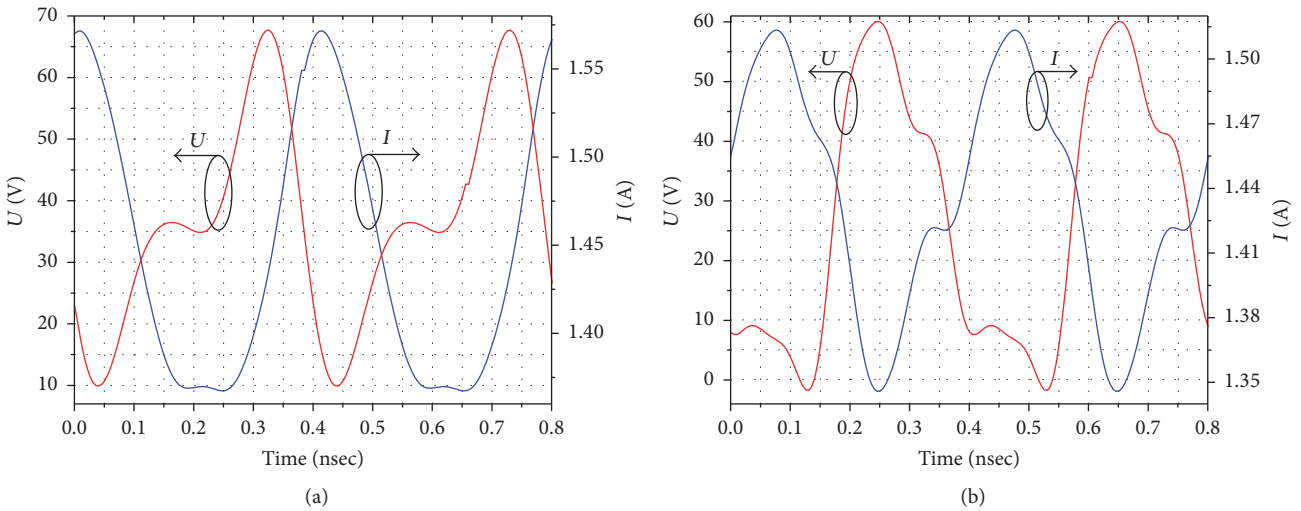

Figure 6: Simulated drain current and voltage time domain waveform for (a) conventional structure and (b) improved structure.

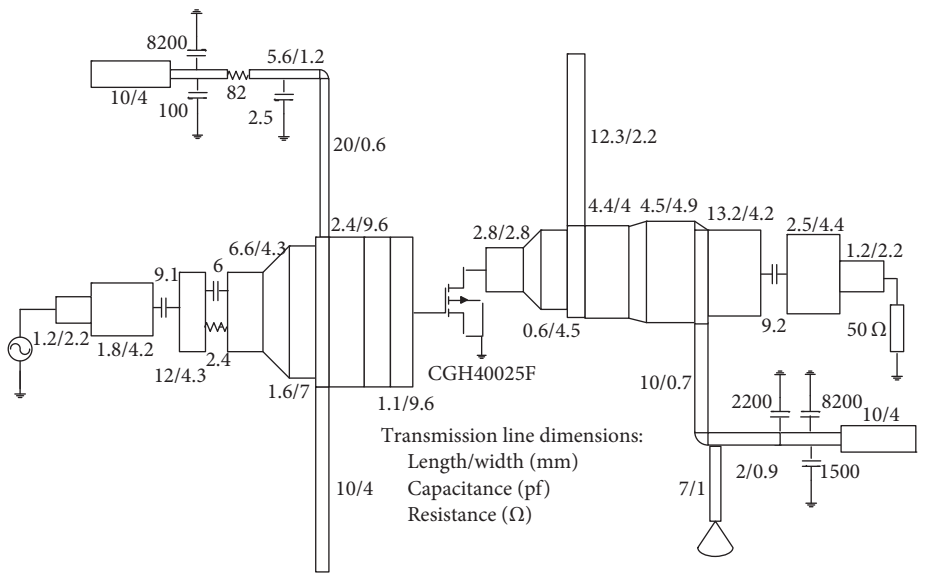

Figure 7: Schematic of the complete power amplifier.

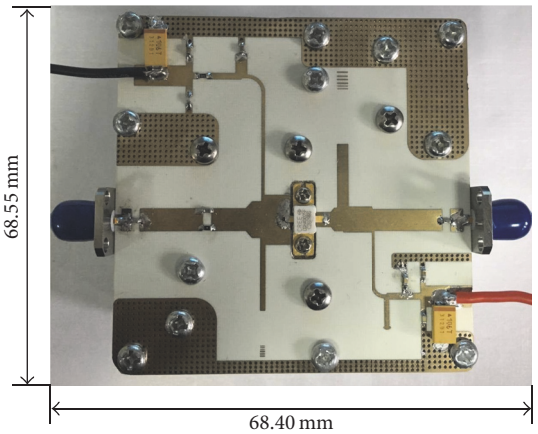

Figure 8: Picture of the fabricated power amplifier.

The drain efficiency and PAE are between 52%–76% and 48.5%–71%, respectively, and the gain is above 10 dB.

The maximum output power measured across the band is 47 dBm at 1.4 GHz while the minimum is 43 dBm at 2.7 GHz. The maximum drain efficiency measured across the band is 76% at 2 GHz with a maximum PAE of 71% at 1.8 GHz. Based on the results above, it is proved that the newly proposed structure is feasible in realizing broadband Class-F power amplifier with high efficiency and high output power.

Measured drain efficiency and gain versus output power at 0.8, 1.7, 2.0, and 2.6 GHz are shown in Figures 11 and 12, respectively. These frequencies are chosen to cover our interested frequency range with 0.8 GHz and 2.6 GHz being the lower and upper frequencies, 1.7 GHz being the center frequency, and 2 GHz being the location where drain efficiency is maximal. The drain efficiency gradually increases with the

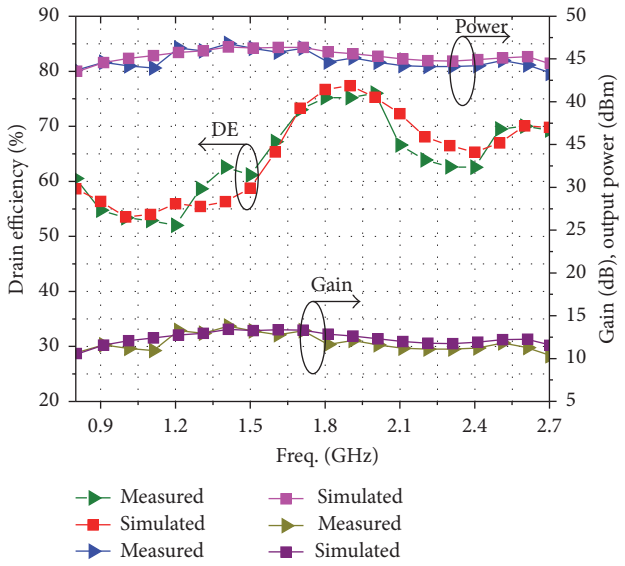

Figure 9: Measured and simulated output power, drive efficiency, and gain versus frequency.

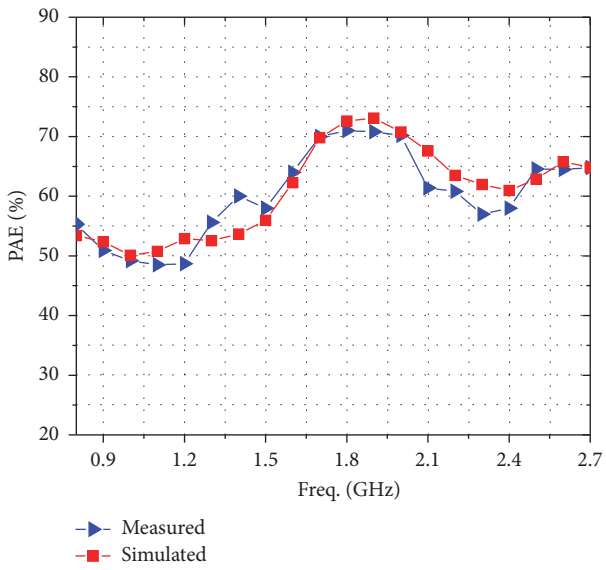

Figure 10: Measured and simulated PAE versus frequency.

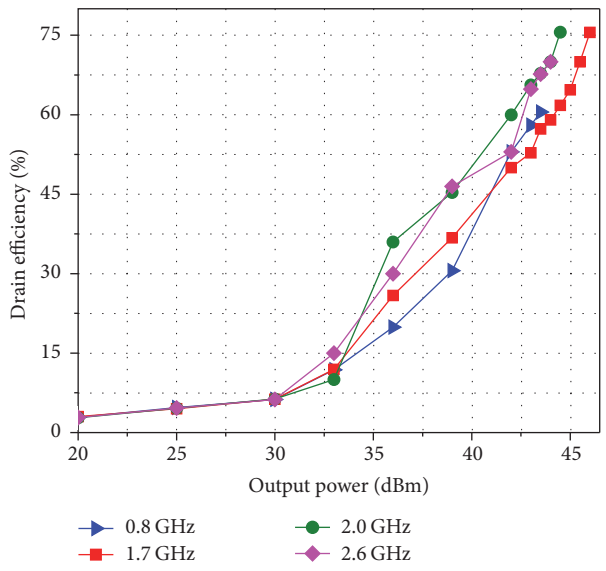

Figure 11: Measured drain efficiency versus output power at 0.8, 1.7, 2.0, and 2.6 GHz.

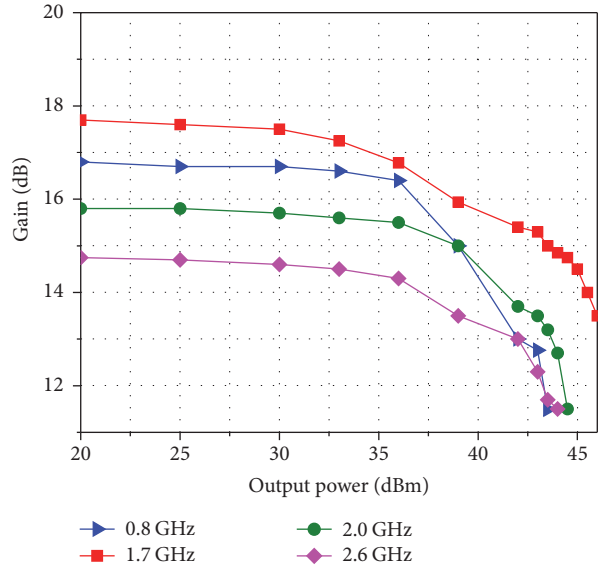

Figure 12: Measured gain versus output power at 0.8, 1.7, 2.0, and 2.6 GHz.

increase of output power as depicted in Figure 11. High drain efficiency can be obtained at high output power.

One can see that when the output power reaches a specific value, the gain begins to drop quickly while the efficiency is increased as shown in Figures 12 and 11. The decrease of gain suggests the loss of linearity. It is also demonstrated that high efficiency and high linearity are so difficult to obtain simultaneously that we have to trade off the design of power amplifiers.

Figure 13 shows the measured and simulated drain efficiency and gain versus output power at 1.7 GHz. When the output power arrives at 43 dBm and above, the gain begins to decline but the efficiency continues to increase. Simulation and measurement agree with each other in the acceptable range.

Figure 14 shows simulated and measured second and third harmonic distortion power levels relative to the fundamental frequency output power. Harmonic suppression level at lower frequencies is not as satisfying as at high frequencies, because the relative test band is wide and harmonics of low frequencies are included in high fundamental frequencies inevitably during measurement. In order to better match the fundamental, we need to compromise on the lower frequency harmonics impedance matching. The second and the third harmonic suppression levels are maintained at −16 to −36 dBc and −16 to −33 dBc, respectively.

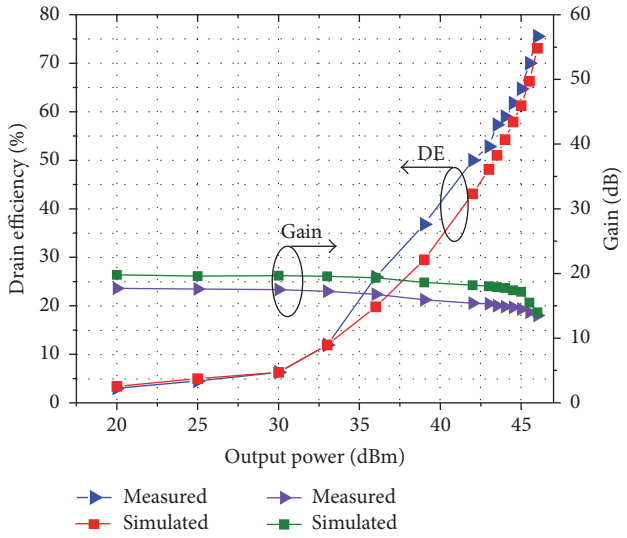

Figure 13: Comparison between measured and simulated drain efficiency and gain versus output power at 1.7 GHz.

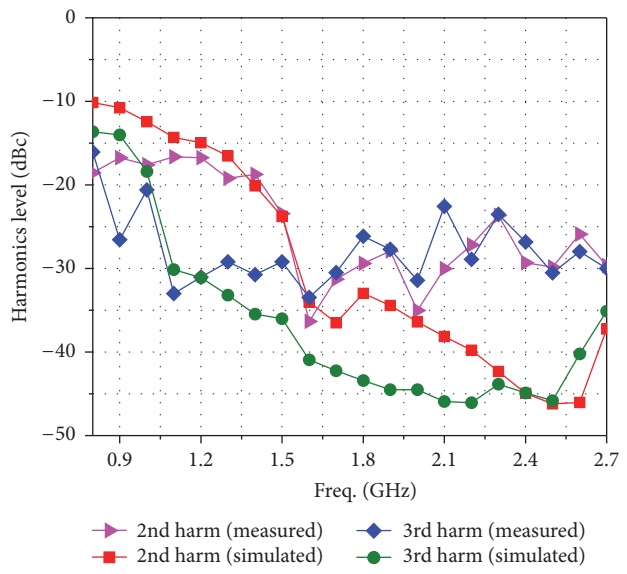

Figure 14: Measured and simulated second and third relative harmonics level. The results are presented relative to the fundamental frequency output power.

4. Conclusions

In this paper, a novel architecture is proposed to compensate the fundamental impedance offset due to package parasitic and suppress harmonics to achieve high efficiency and high output power. The feasibility of the structure was verified by measurement results. The measured results show that the relative bandwidth is 109% in the range of 0.8–2.7 GHz, the saturated output power is over 43 dBm, the average efficiency is more than 60%, and the gain is above 10 dB. The results manifest remarkable advantages over traditional Class-F power amplifiers.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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